



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Description

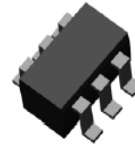
Dual-rail clamp diodes are designed to provide ESD protection for high speed data interfaces. They are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading.

The UMDRV05UL-4 consists of four pairs of diodes in series which steer the positive or negative ESD current pulse to either the positive (Vp) or negative (Vn) supply rail, and a TVS diode which is embedded between Vp and Vn. The ultra low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The TVS diode prevents over-voltage on the power line, protecting any down stream components.

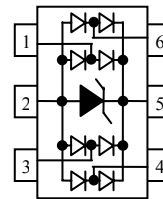
Features

- * Solid-state silicon avalanche technology
- * SOT23-6L package
- * Bi-Directional protection
- * Protects up to four data lines and one power line
- * Ultra Low channel input capacitance of 0.8pF
- * Working voltage: 5V
- * Low clamping factor V_{cl}/V_{br}
- * Low leakage current
- * Full RoHS compliance
- * Complies with the following standards:
 - IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
 - IEC 61000-4-4 (EFT) (5/50ns)
 - IEC 61000-4-5 (Surge) (8/20µs)

Ultra Low Capacitance Series TVS



SOT23-6L Pin Configuration



<u>Pin</u>	<u>Description</u>
1	I/O
2	Vn
3	I/O
4	I/O
5	Vp
6	I/O

Mechanical Characteristics

- * Molded SOT23-6L package
- * Weight 16 milligrams (Approximate)
- * Available in Lead-Free Pure-Tin Plating
- * Solder Reflow Temp: Pure-Tin (Sn), 260-270°C
- * Consult Factory for Leaded Device Availability
- * Flammability Rating UL 94V-0
- * 8mm Tape and Reel per EIA Standard 481
- * Device Marking: Marking Code,
Pin one defined by DOT

Applications

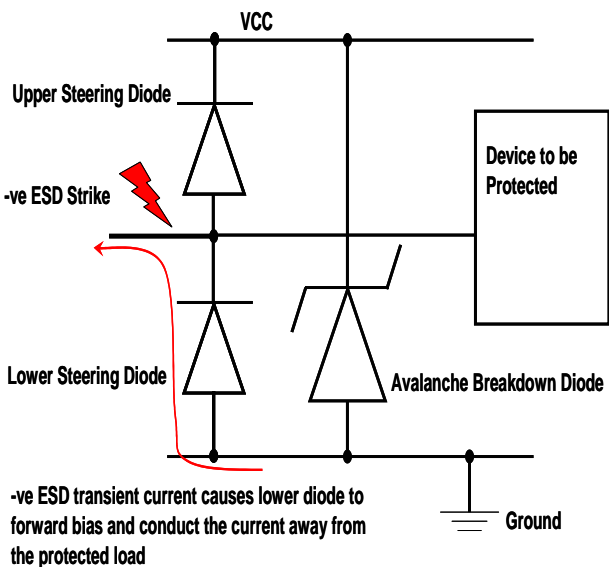
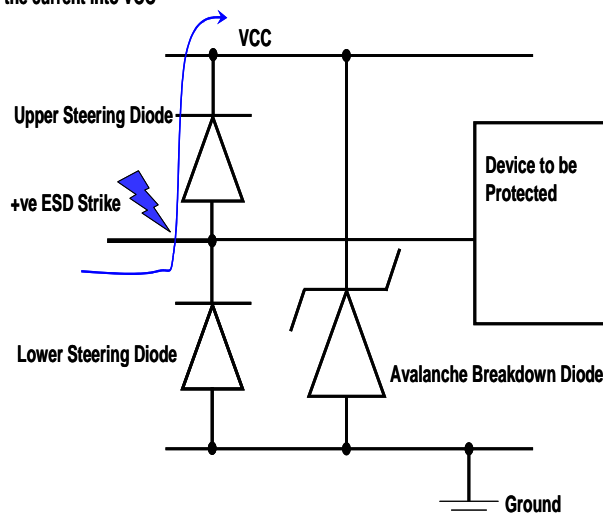
- * Handset Sim Card and I/O Port Protection
- * VGA (D-sub) Port Protection
- * 10/100/1000 Ethernet Port Protection
- * USB2.0 Power and Data Line Protection
- * IEEE1394 Firewire Port Protection
- * Digital Camera
- * Set Top Boxes and Digital TV

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection
Absolute Maximum Ratings @ 25°C unless otherwise specified

Parameter	Symbol	Value	Units
Peak Pulse Power; pulse waveform = 8/20μs	Ppp	200	W
Peak Pulse Current; pulse waveform = 8/20μs	Ipp	5.4	A
ESD per IEC 61000-4-2 (Air)	Vpp	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature	Tj	-77 to 345	°C
Storage Temperature	Tstg	-55 to 150	°C

Dual-Rail Clamp Diode Protection

+ve ESD transient current causes upper diode to forward bias and conduct the current into VCC

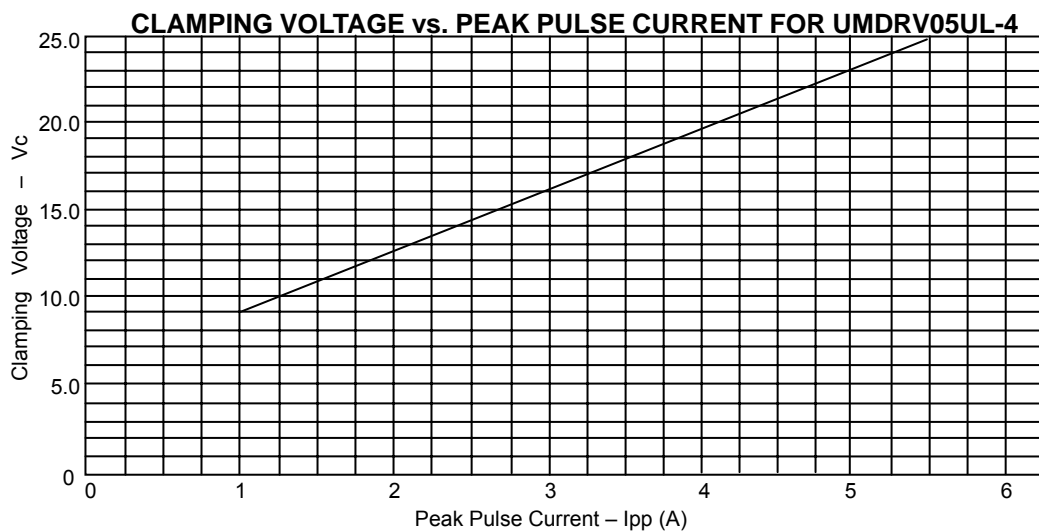
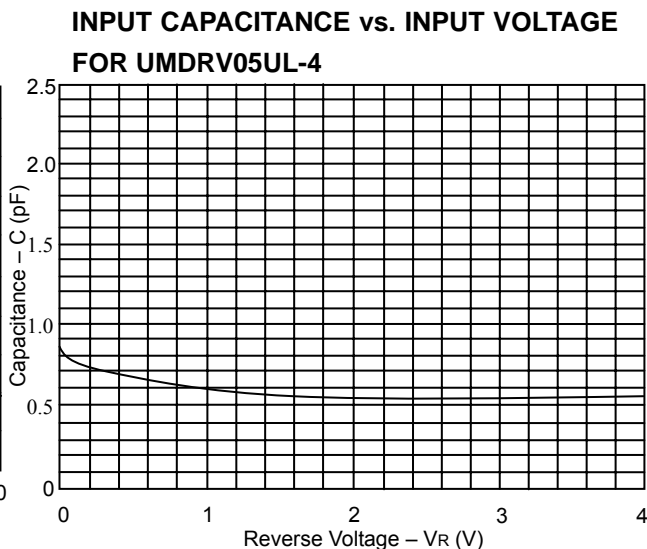
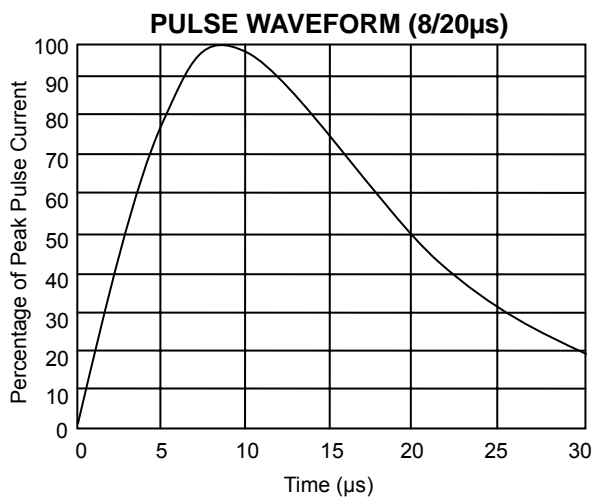
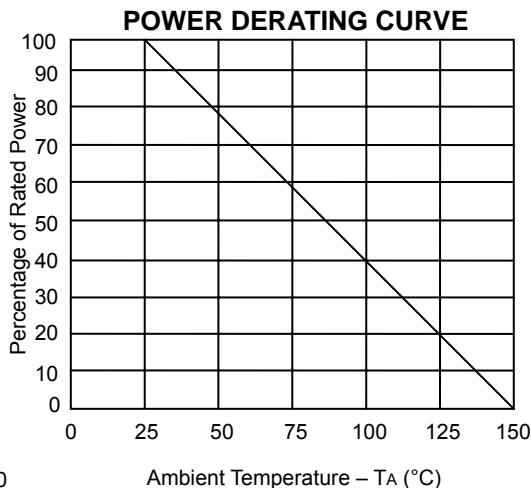
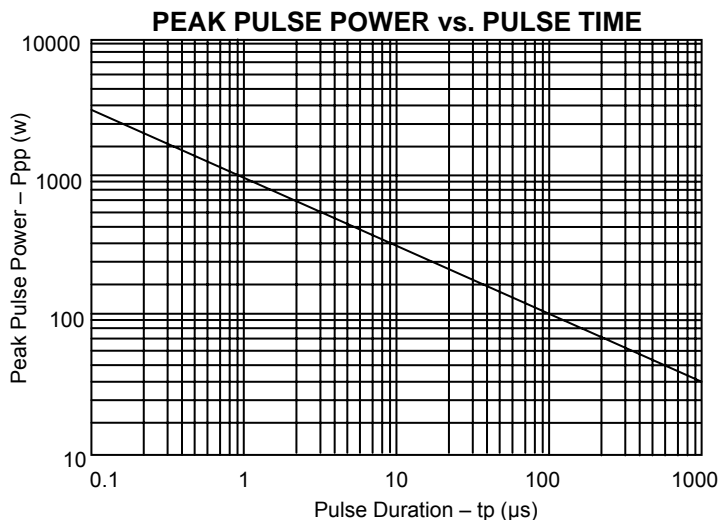

Electrical Characteristics @ 25°C unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operating Supply Voltage (Vp)			3.3	5.5	V
Operating Supply Current (Ip)	Vp=3.3v			8	μA
Forward Voltage Top Diode	If=8mA	0.6	0.8	0.95	V
Forward Voltage Bottom Diode		-0.6	-0.8	-0.95	V
Leakage Current	Vp=5v		±0.1	±1	μA
Signal Clamp Voltage	Ipp=10mA	6.5	7.5	9.0	V
Clamping Voltage +ve Transient	Ipp=1A, Tp=8/20μs		9		V
Clamping Voltage -ve Transient			-1.5		V
Input Capacitance @1MHz	Vp=3.3v, Vi/o=1.65v	0.6	0.8	1.0	pF



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Electrical Characteristics Graphs



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

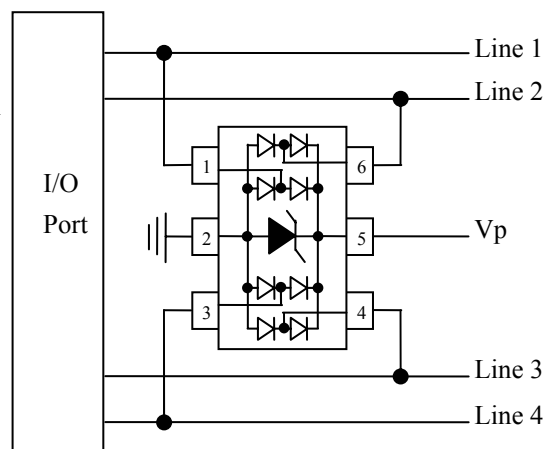
Applications Information

The UMDRV05UL-4 has a ultra low typical capacitance of 0.8pF and operates with virtually no insertion loss to 1GHz. This makes the device ideal for protection of high-speed data lines such as USB2.0, Firewire, DVI and gigabit Ethernet interfaces. The UMDRV05UL-4 is designed for use in applications where board space is at a premium. Each device requires less than 8.6mm² of PCB area and will protect up to four data lines and one power line.

To protect data lines and the power line, connect pin 5 directly to the positive supply rail (Vp). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.

Circuit connectivity is as follows:

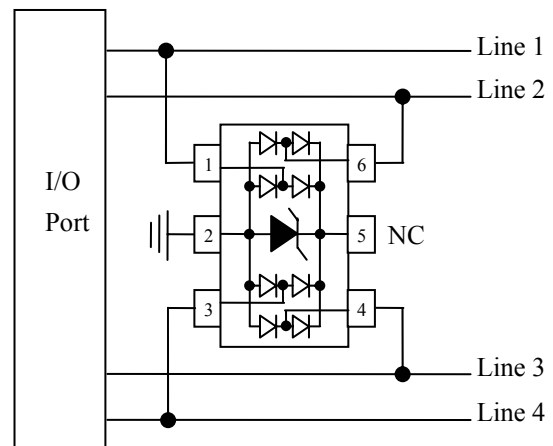
- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 6
- Line 3 is connected to Pin 4
- Line 4 is connected to Pin 3
- Pin 5 is connected to Vp
- Pin 2 is connected to ground



In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

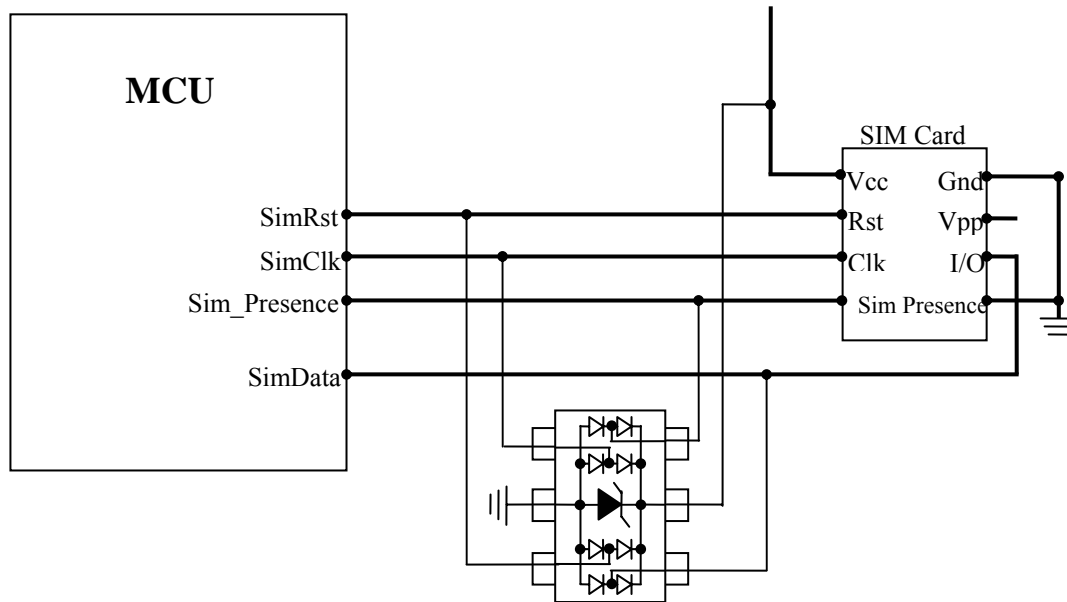
Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 6
- Line 3 is connected to Pin 4
- Line 4 is connected to Pin 3
- Pin 5 is not connected
- Pin 2 is connected to ground

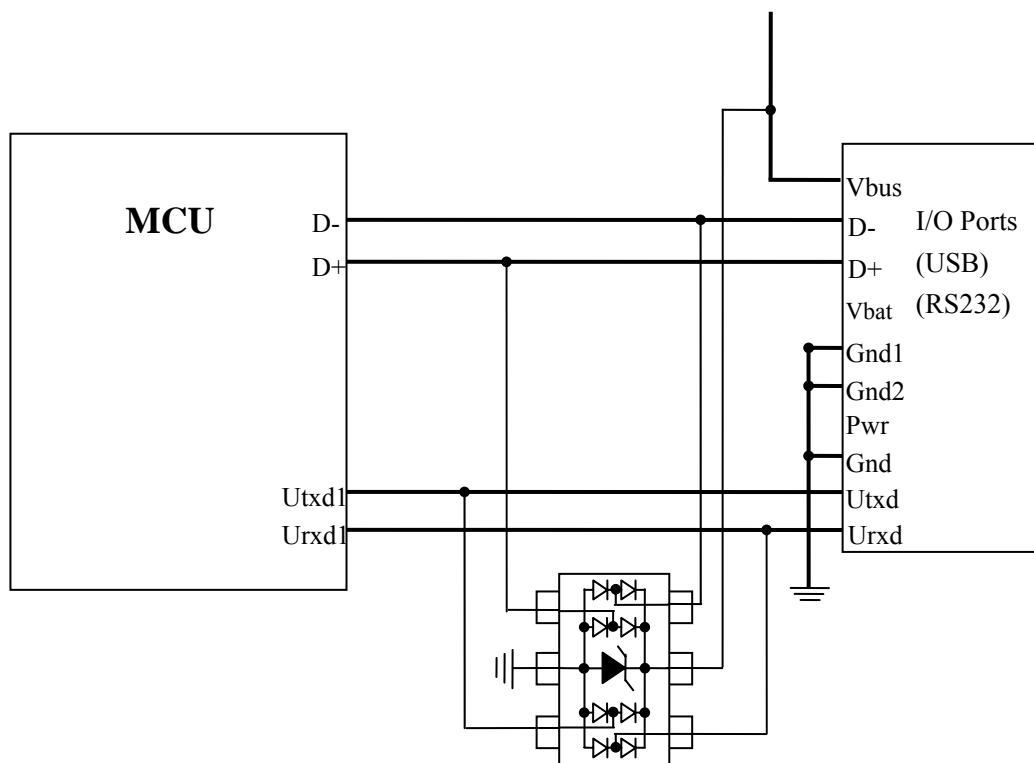


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMDRV05UL-4 on Handset Sim Card Port Application



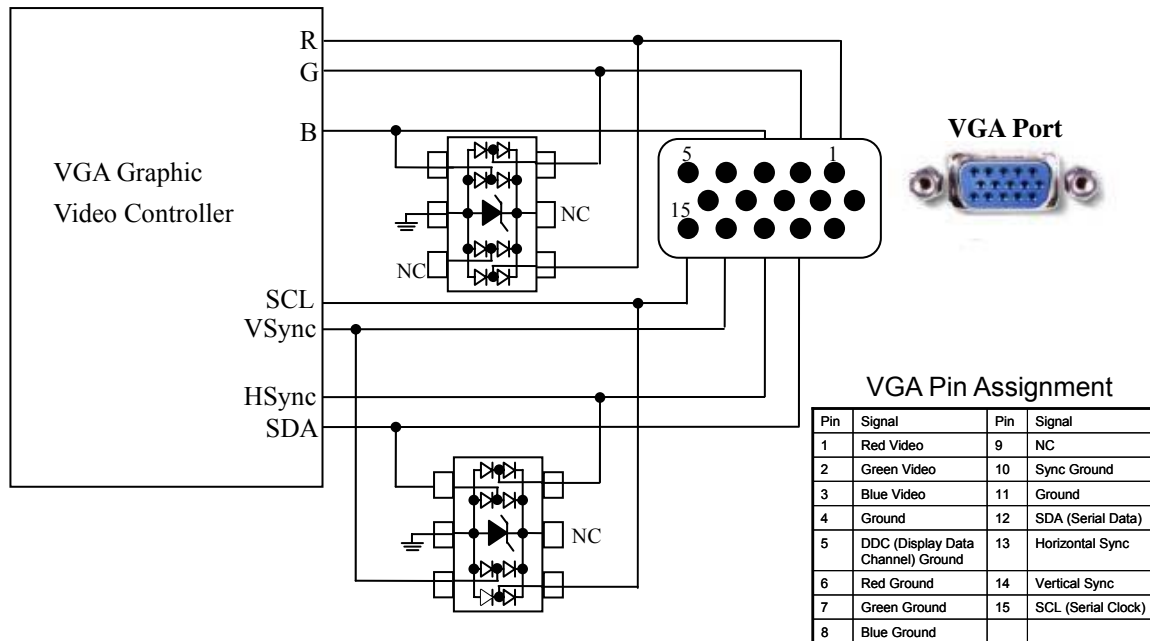
UMDRV05UL-4 on Handset I/O Port Application



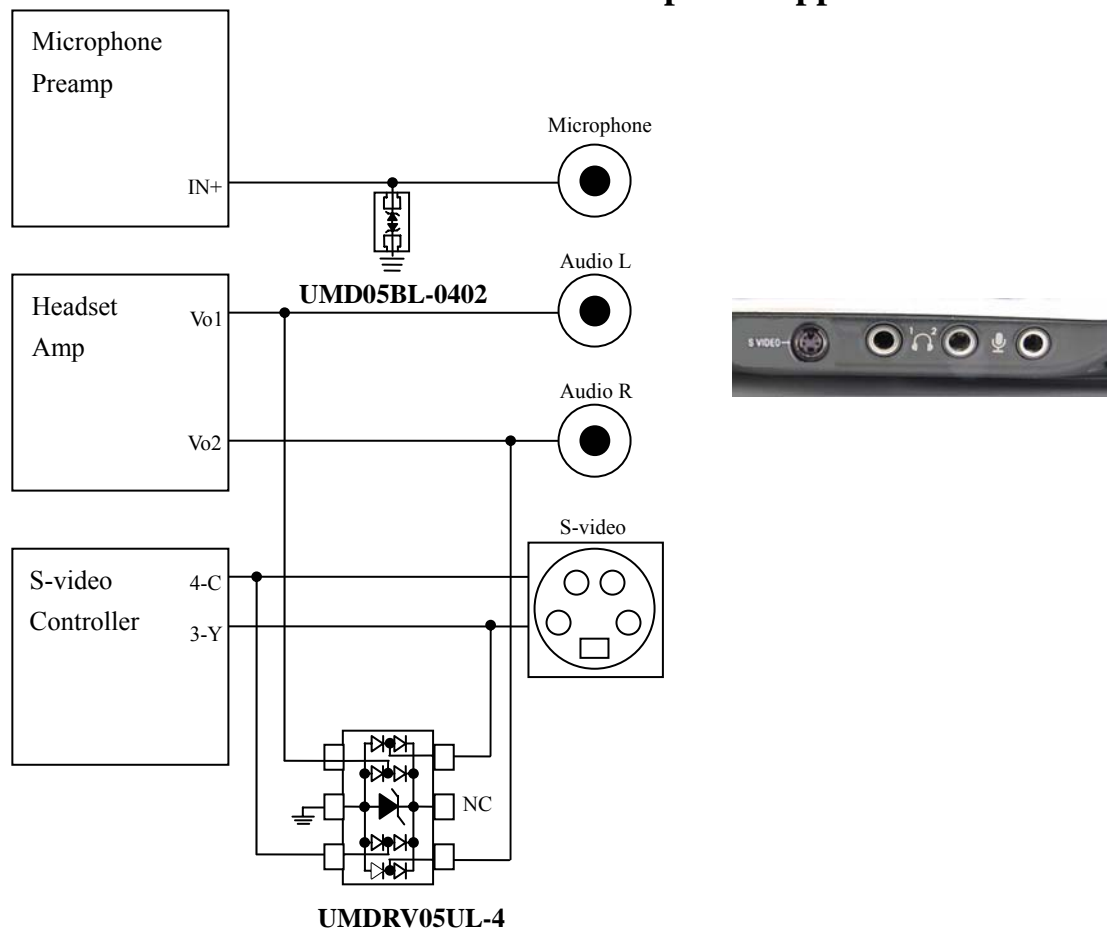


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMDRV05UL-4 on VGA Port Application

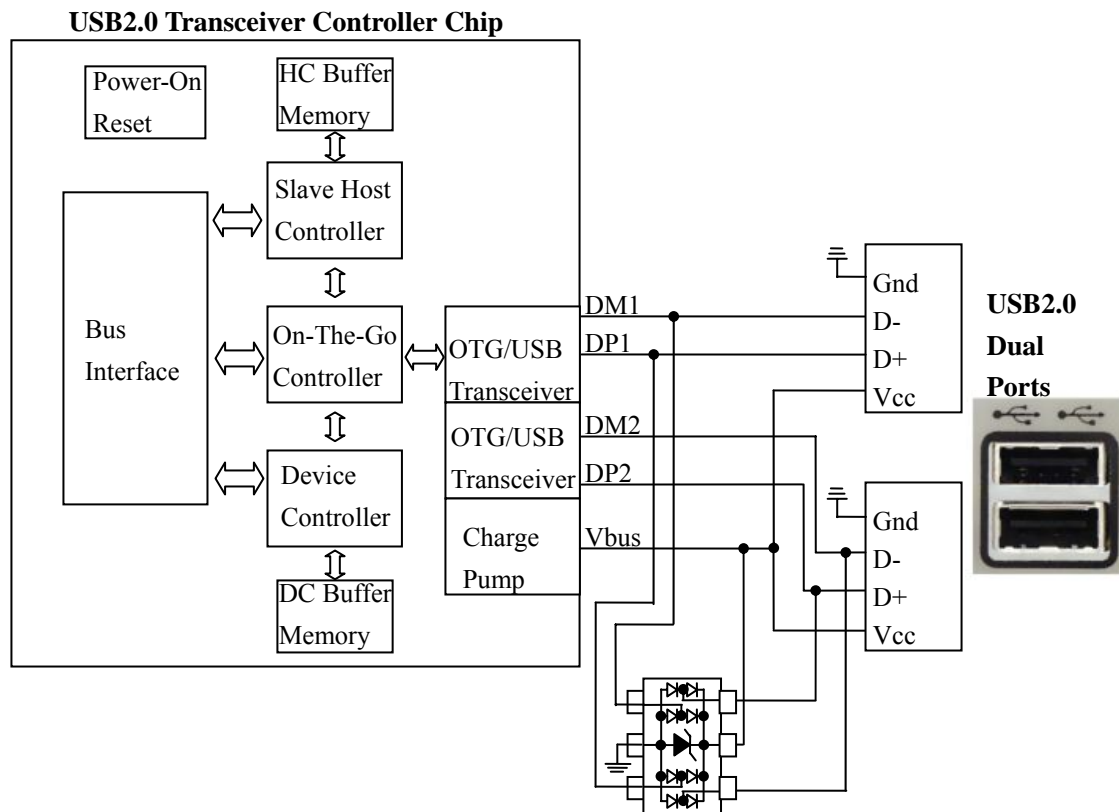


UMDRV05UL-4 on S-video/Audio/Microphone Application

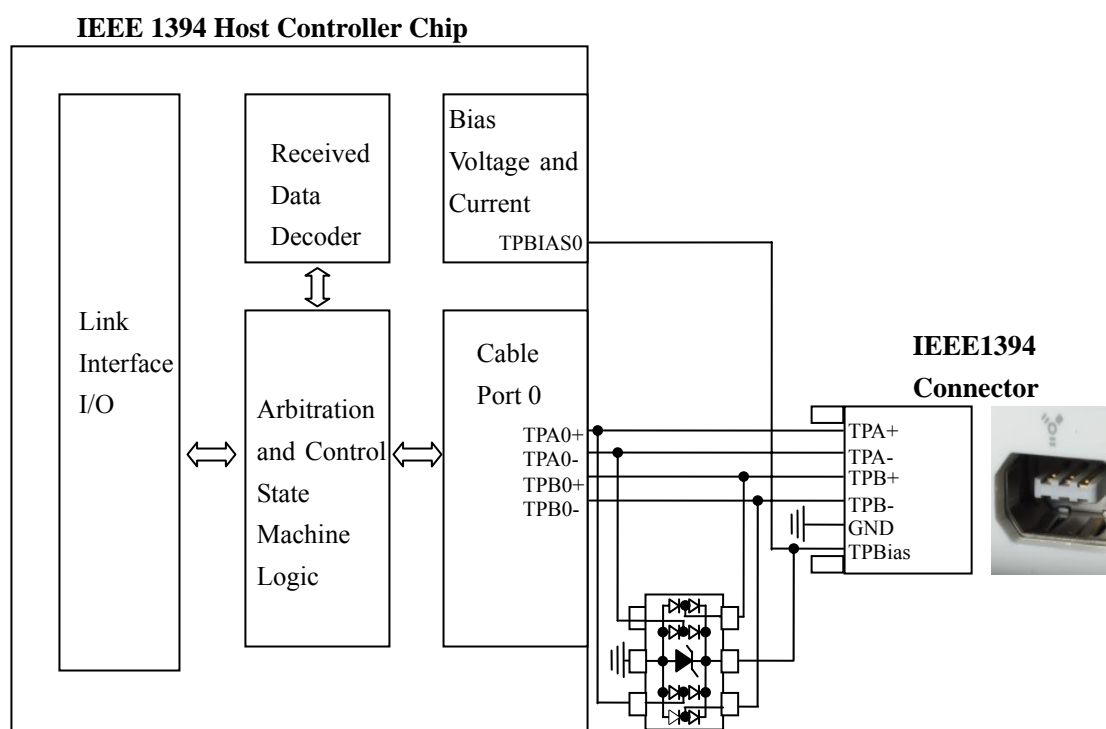


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMDRV05UL-4 on Dual USB2.0 Ports Application



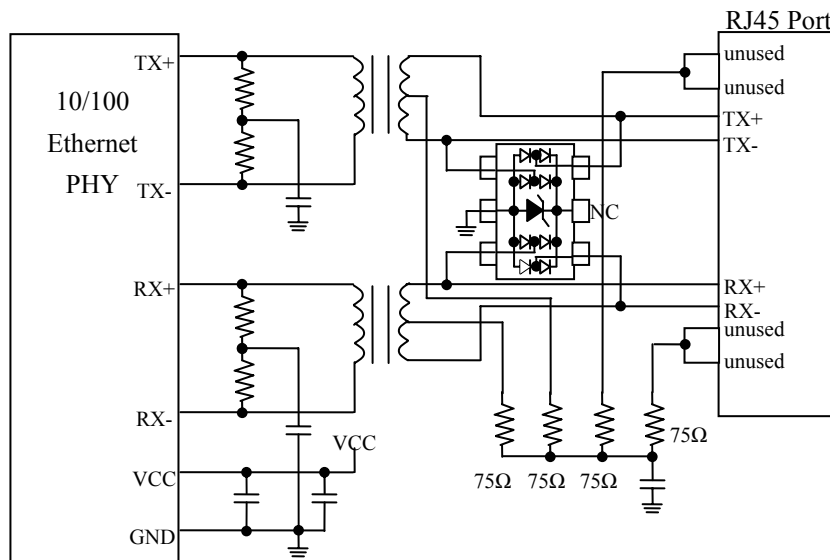
UMDRV05UL-4 on IEEE1394 Connector Application



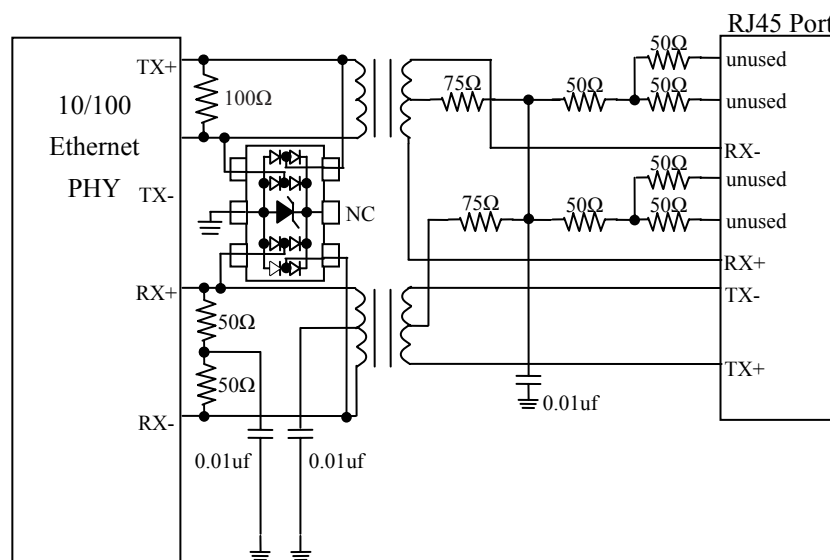


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMDRV05UL-4 on 10/100 Ethernet Application (Option A)



UMDRV05UL-4 on 10/100 Ethernet Application (Option B)



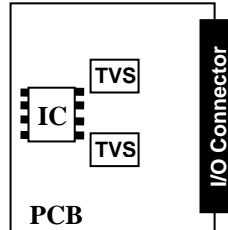
4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Circuit Board Layout Recommendations

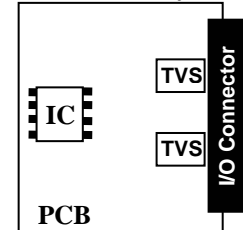
Good circuit board layout is critical for creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

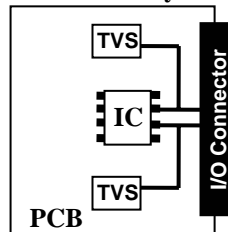
Poor PCB Layout



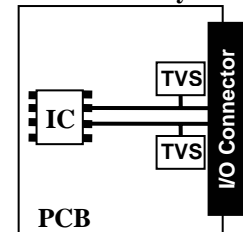
Good PCB Layout



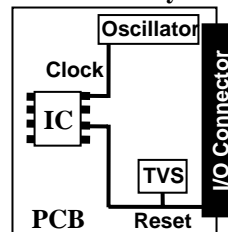
Poor PCB Layout



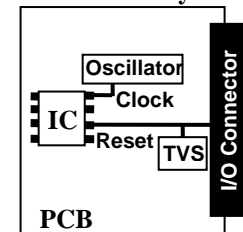
Good PCB Layout



Poor PCB Layout



Good PCB Layout



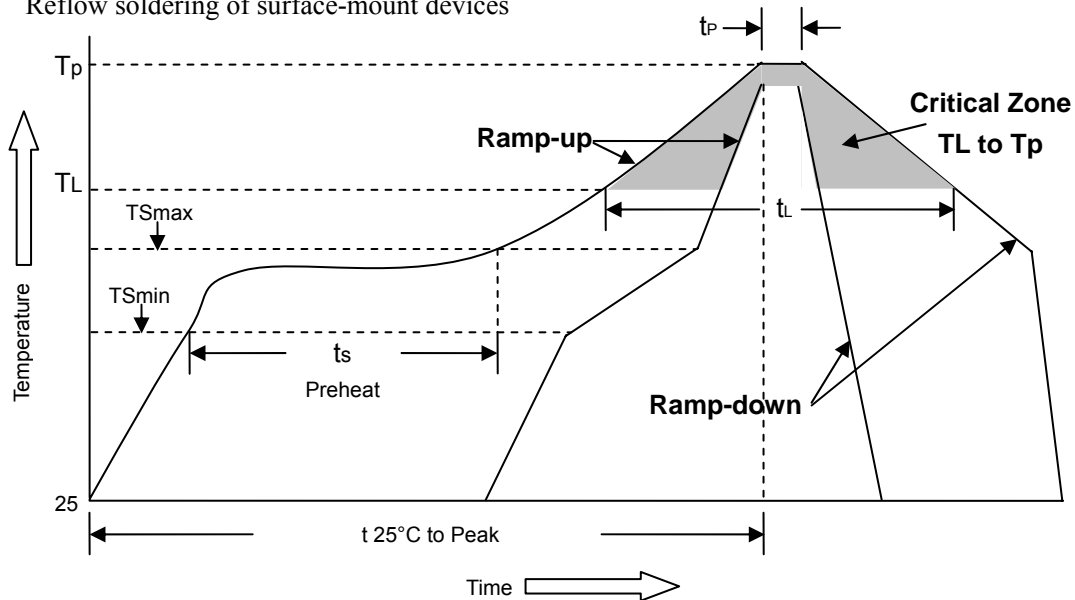
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

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Soldering Method for UMD's Products

1. Storage environment: Temperature = 10°C~35°C Humidity = 65%±15%
2. Reflow soldering of surface-mount devices



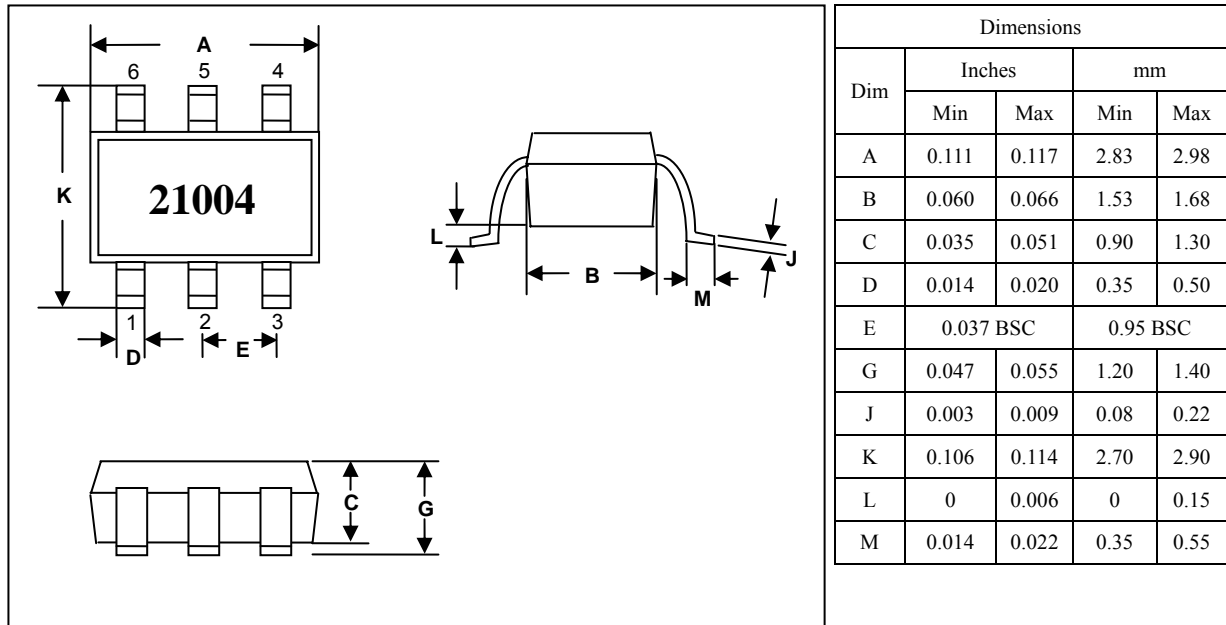
Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec
Preheat	
- Temperature Min (TSmin)	150°C
- Temperature Max (TSmax)	200°C
- Time (min to max) (ts)	60~180sec
TSmax to TL	
- Ramp-up Rate	<3°C/sec
Time maintained above:	
- Temperature (TL)	220°C
- Time (tL)	50~145sec
Peak Temperature (Tp)	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	20~40sec
Ramp-down Rate	<6°C/sec
Time 25°C to peak Temperature	<8 minutes

Flow (wave) soldering (solder dipping)

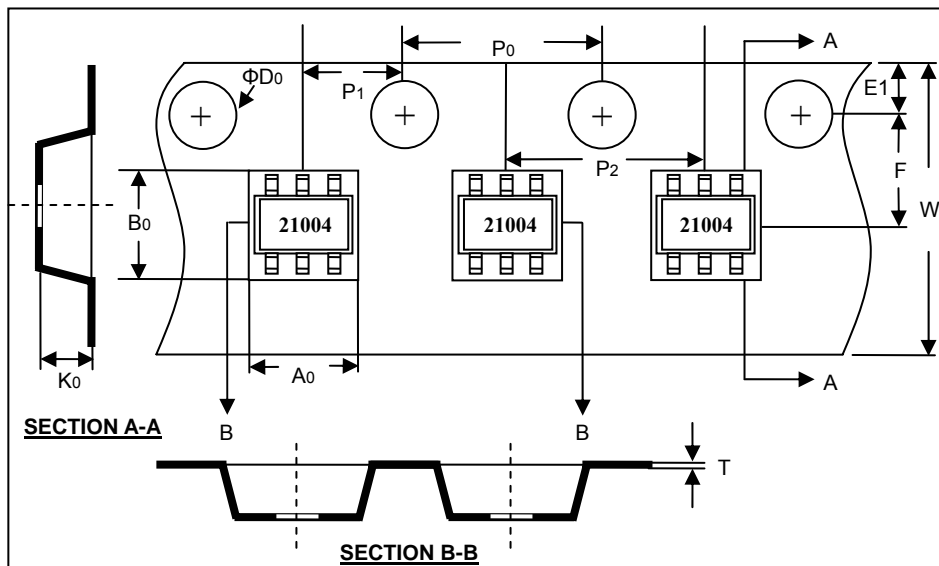
Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec

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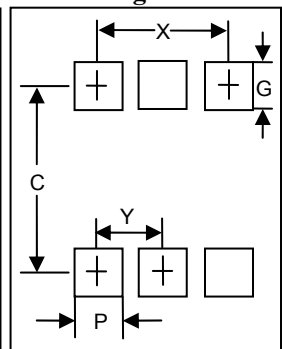
SOT23-6L Dimension Drawing



SOT23-6L Carrier Dimension



Mounting Pattern



Typical		
Dim	MM	Inches
C	2.40	0.094
Y	0.95	0.037
P	0.70	0.028
G	1.00	0.039
X	1.90	0.075

Dimensions in mm.

Reel Dia.	Tape Width	A0	B0	K0	ΦD0	E1
178mm (7")	8mm	3.20±0.10	3.20±0.10	1.65±0.10	1.50±0.10	1.75±0.10
F	W	P0	P1	P2	T	
3.50±0.05	8.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25±0.02	



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Marking Code

Part Number	Device Marking
UMDRV05UL-4	21004

Ordering Information

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMDRV05UL-4	Pb-Free	3,000	7 inch

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