

Bidirectional TVS Array for Protection of Eight Lines

PRODUCT DESCRIPTION

The UMDA05B-8 series of transient voltage suppressors are designed to protect components which are connected to data and transmission lines from voltage surges caused by electrostatic discharge (ESD), electrical fast transients (EFT), and lightning.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The UMDA05B-8 is designed to provide transient suppression on multiple data lines and I/O ports. The low profile SO-14 design allows the user to protect up to eight data and I/O lines with one package. They are bidirectional device and may be used on lines where the normal operating voltage is above and below ground (i.e. -12V to +12V).

The UMDA05B-8 TVS diode array will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

FEATURES

- ✧ Transient protection for data lines to
IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 12A (8/20 μs)
- ✧ Small SO-14 surface mount package
- ✧ Protects eight I/O lines
- ✧ Working voltages: 5V
- ✧ Low leakage current
- ✧ Low operating and clamping voltages
- ✧ Solid-state silicon avalanche technology

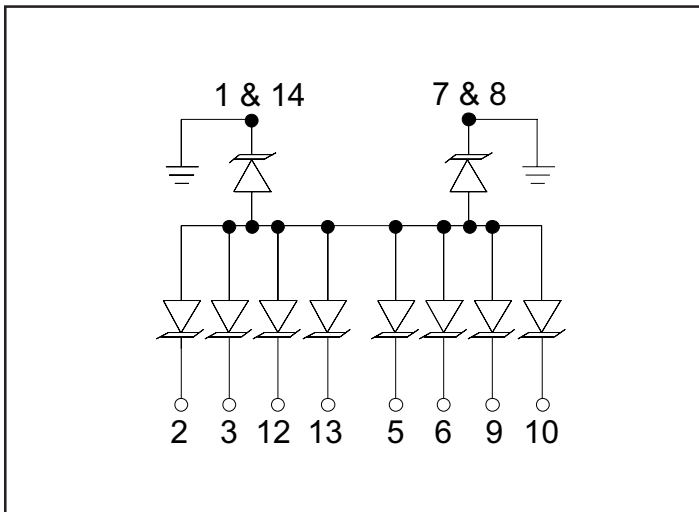
Mechanical Characteristics

- ✧ JEDEC SO-14 package
- ✧ Molding compound flammability rating: UL 94V-0
- ✧ Marking : Part Number, Logo, Date Code
- ✧ Packaging : Tape and Reel per EIA 481

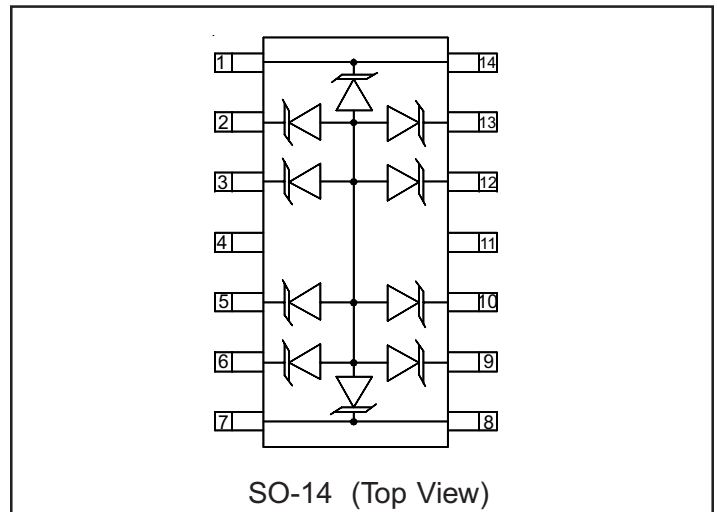
Applications

- ✧ RS-232 and RS-422 Data Lines
- ✧ Microprocessor Based Equipment
- ✧ LAN/WAN Equipment
- ✧ Set-Top Box
- ✧ Notebooks, Desktops, and Servers
- ✧ Portable Instrumentation
- ✧ Peripherals
- ✧ Serial and Parallel Ports

Circuit Diagram



Schematic & PIN Configuration



Bidirectional TVS Array for Protection of Eight Lines

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	300	Watts
Lead Soldering Temperature	T_L	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_J	-55 to +125	$^{\circ}C$
Storage Temperature	T_{STG}	-55 to +150	$^{\circ}C$

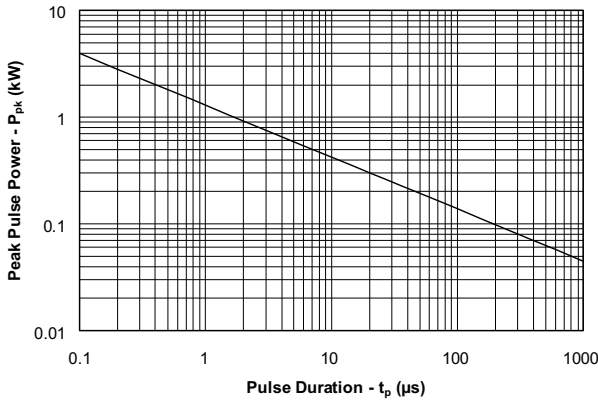
Electrical Characteristics

UMDA05B-8						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^{\circ}C$			20	μA
Clamping Voltage	V_C	$I_{PP} = 1A, t_p = 8/20\mu s$			9.8	V
Peak Pulse Current	I_{PP}	$t_p = 8/20\mu s$			17	A
Junction Capacitance	C_j	Between I/O Pins and Ground $V_R = 0V, f = 1MHz$			350	pF

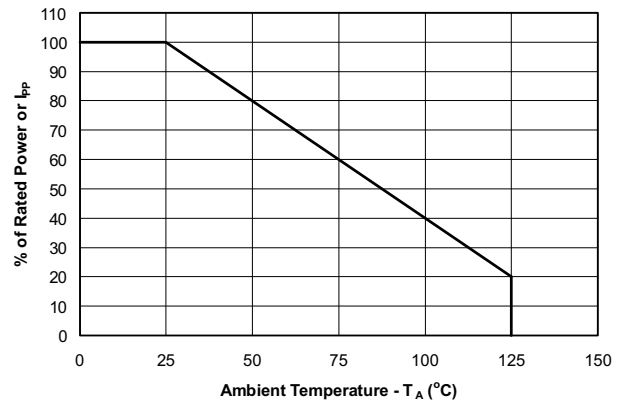
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Typical Characteristics

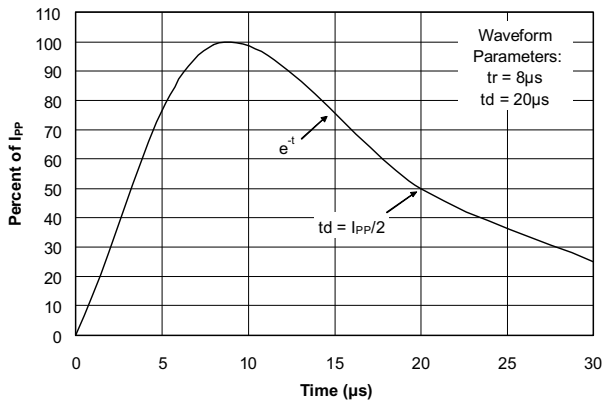
Non-Repetitive Peak Pulse Power vs. Pulse Time



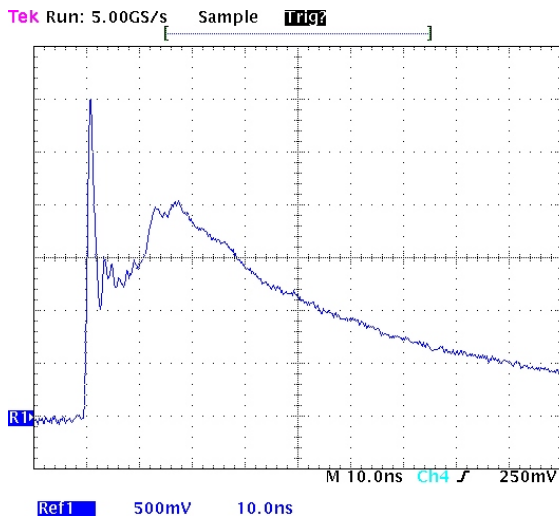
Power Derating Curve



Pulse Waveform



ESD Pulse Waveform (IEC 61000-4-2)



IEC 61000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30 ns (A)	Peak Current at 60 ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

Bidirectional TVS Array for Protection of Eight Lines

Device Connection for Protection of Eight Data Lines

The UMDA05B-8 is designed to protect up to 8 data or I/O lines. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

The UMDA05B-8 TVS arrays employ a monolithic structure. Therefore, the working voltage (V_{RWM}) and breakdown voltage (V_{BR}) specifications apply to the differential voltage between any two data line pins. For example, the UMDA05B-8 is designed for a maximum voltage excursion of $\pm 12V$ between any two data lines.

The device is connected as follows:

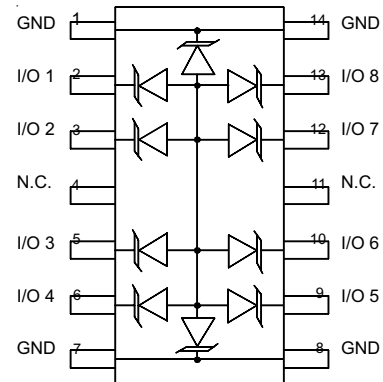
- Pins 2, 3, 5, 6, 9, 10, 12 and 13 are connected to the lines that are to be protected. Pins 1, 7, 8, and 14 are connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces. Pins 4 and 11 are not connected.

Circuit Board Layout Recommendations for Suppression of ESD.

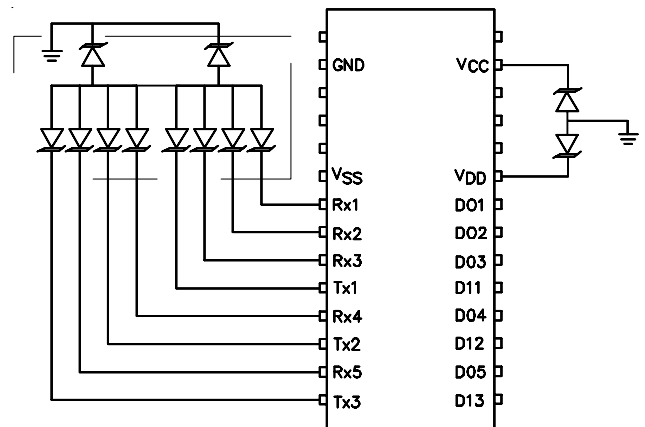
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Circuit Diagram

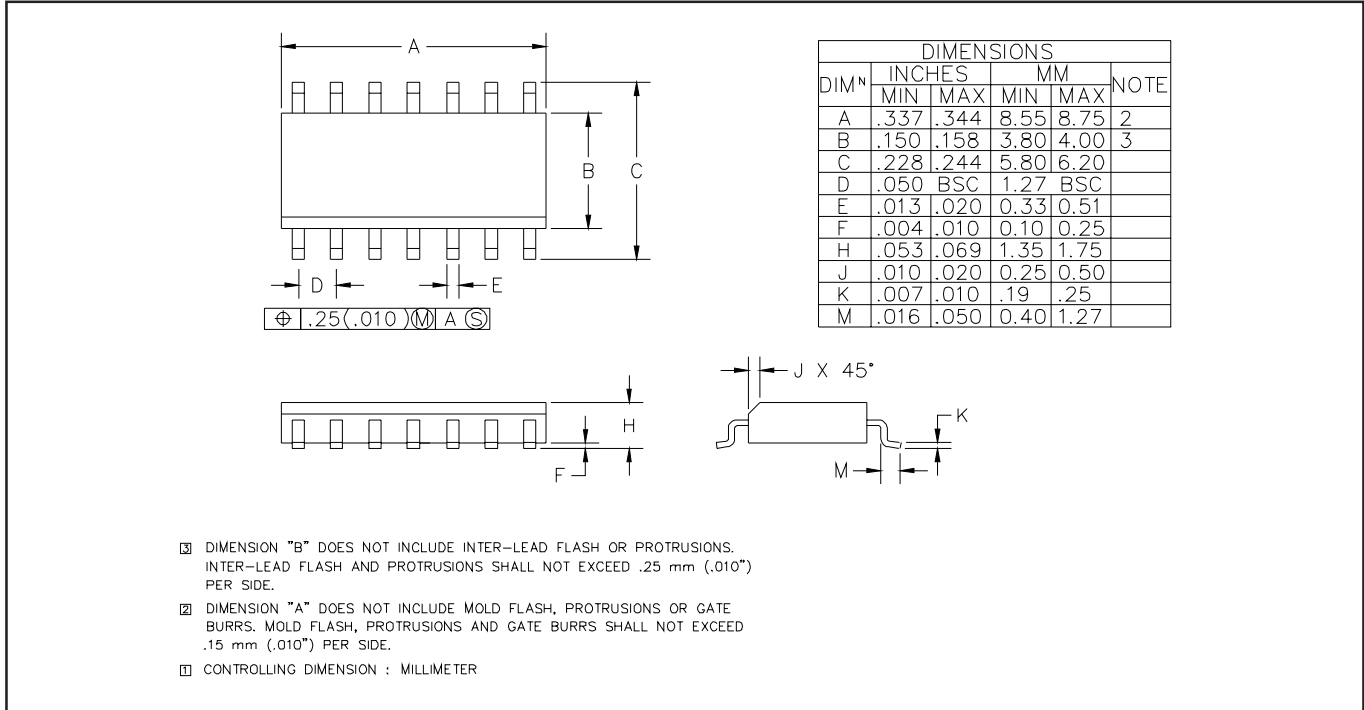


Connection Diagram



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Outline Drawing - SO-14



Land Pattern - SO-14

