



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Description

Dual-rail clamp diodes are designed to provide ESD protection for high speed data interfaces. They are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading.

The UMD0524P consists of four pairs of diodes in series, and a TVS diode is embedded inside the package. It has a typical capacitance of only 0.30pF between I/O pins. This allows it to be used on circuits operating in excess of 3GHz without signal attenuation. They are designed for easy PCB layout by allowing the traces to run straight through the device. The combination of small size, low capacitance, and high level of ESD protection becomes a flexible solution for applications such as HDMI, MDDI and Serial ATA.

Features

- * Dual-Rail Clamp technology
* DFN-10 package
* Bi-Directional protection
* Protects four data lines
* Low input capacitance 0.3pF typical (I/O to IO)
* Working voltage: 5V
* Low clamping factor Vcl/Vbr
* Low leakage current
* Full RoHS compliance
* Complies with the following standards:
- IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
- IEC 61000-4-4 (EFT) (5/50ns)
- IEC 61000-4-5 (Surge) (8/20µs)

Ultra Low Capacitance Series TVS



DFN-10 Pin Configuration

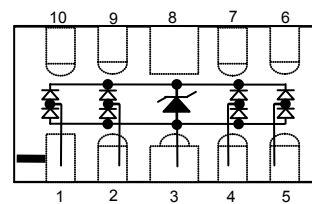


Table with 2 columns: Pin and Description. Pin 1, 2, 4 and 5 are Input Lines; Pin 6, 7, 9 and 10 are Output Lines; Pin 3 is Ground.

Mechanical Characteristics

- * Molded DFN-10 package
* Available in Lead-Free Pure-Tin Plating
* Solder Reflow Temp: Pure-Tin (Sn), 260-270°C
* Consult Factory for Leaded Device Availability
* Flammability Rating UL 94V-0
* 8mm Tape and Reel per EIA Standard 481
* Device Marking: Marking Code, Pin one defined by Line

Applications

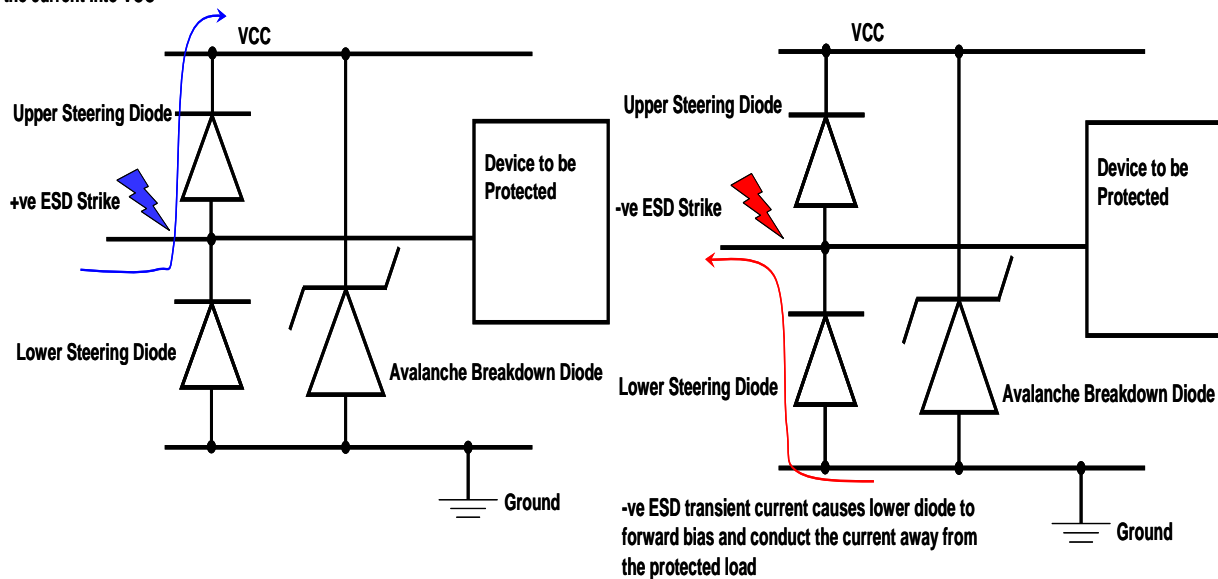
- * HDMI Port Protection
* DVI Port Protection
* VGA and SCART Ports Protection
* MDDI Ports Protection
* Notebook Computers
* Set Top Boxes and Digital TV
* Serial ATA and PCI Express

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection
Absolute Maximum Ratings @ 25°C unless otherwise specified

Parameter	Symbol	Value	Units
Peak Pulse Power; pulse waveform = 8/20µs	P _{pp}	150	W
Peak Pulse Current; pulse waveform = 8/20µs	I _{pp}	3	A
ESD per IEC 61000-4-2 (Air)	V _{pp}	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature	T _j	-55 to 125	°C
Storage Temperature	T _{stg}	-55 to 150	°C

Dual-Rail Clamp Diode Protection

+ve ESD transient current causes upper diode to forward bias and conduct the current into VCC

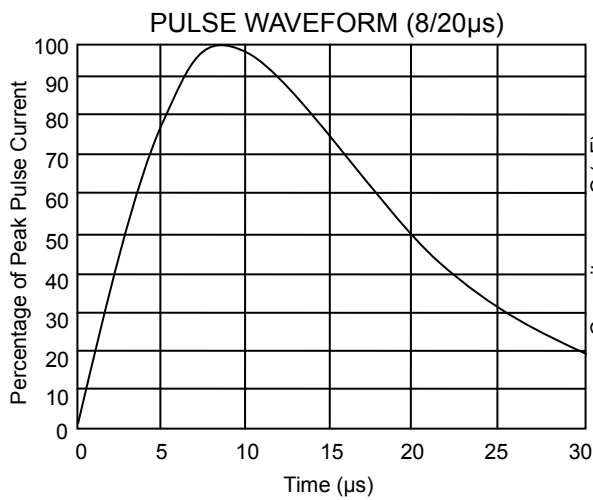
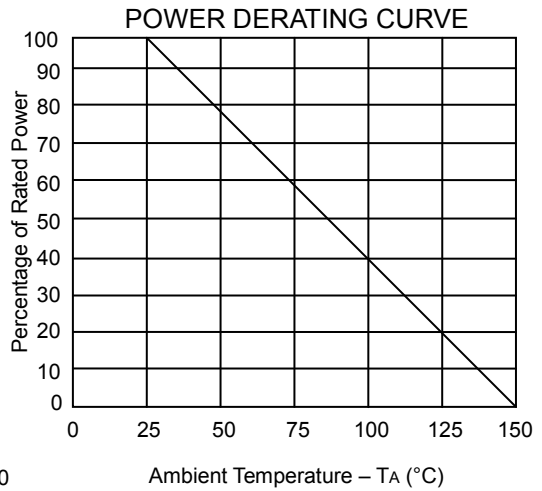
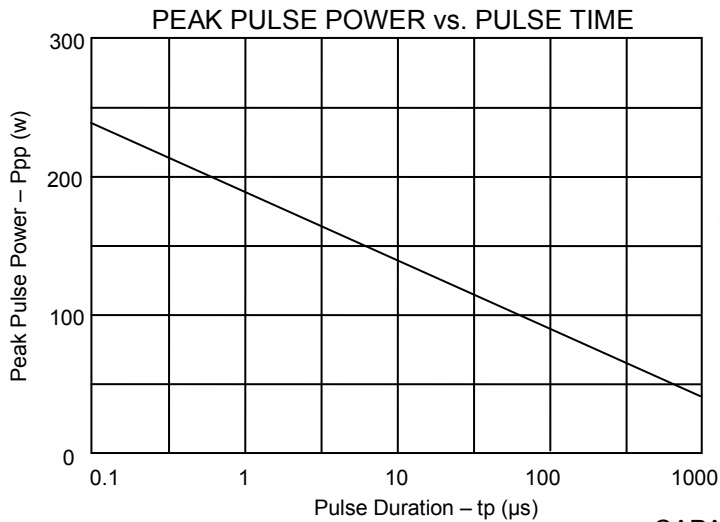

Electrical Characteristics @ 25°C unless otherwise specified

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Stand-off Voltage	V _{wm}	Any I/O to ground			5.0	V
Breakdown Voltage	V _{br}	I _t =1mA, Any I/O to ground	8.5			V
Leakage Current	I _r	V _{wm} =5V Any I/O to ground		0.0005	1	µA
Clamping Voltage	V _c	I _{pp} =1A, T _p =8/20µs I _{pp} =3A, T _p =8/20µs Any I/O to ground			9.8 12.0	V
Junction Capacitance	C _j	V _r =0V, f=1MHz I/O to I/O		0.3	0.4	pF
		V _r =0V, f=1MHz I/O to Gnd		0.6	0.8	

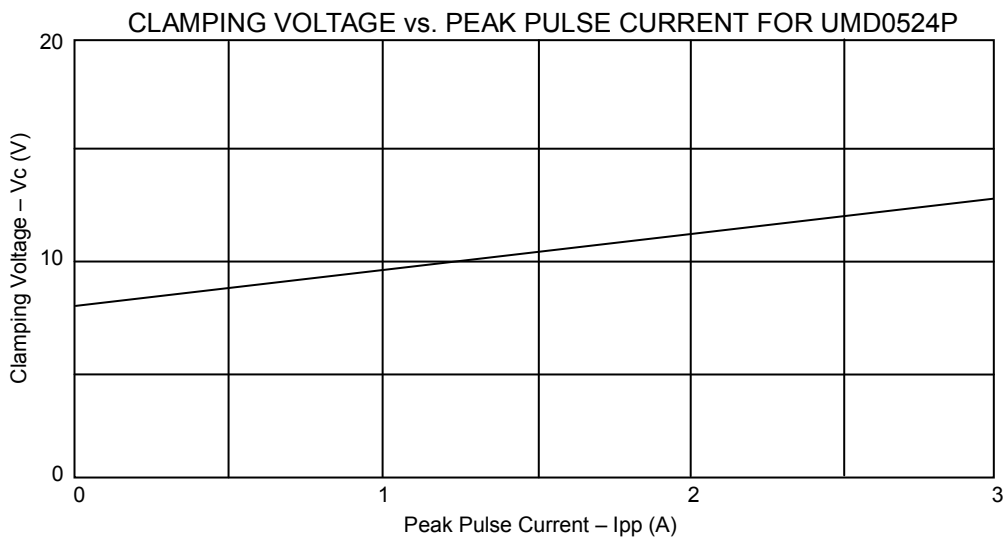
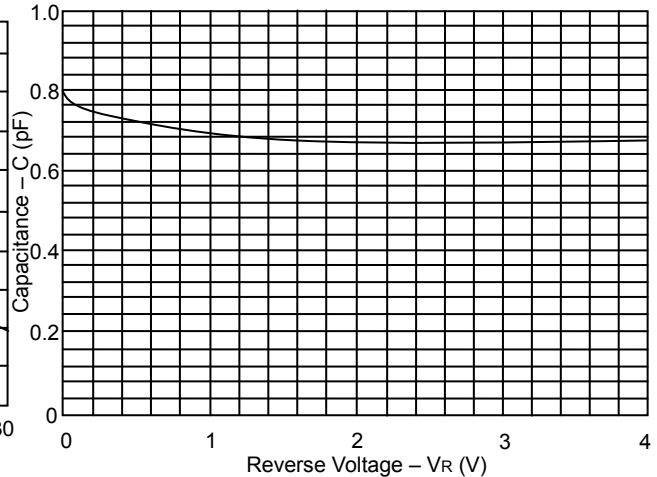


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Electrical Characteristics Graphs



CAPACITANCE vs. REVERSE VOLTAGE FOR UMD0524P



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

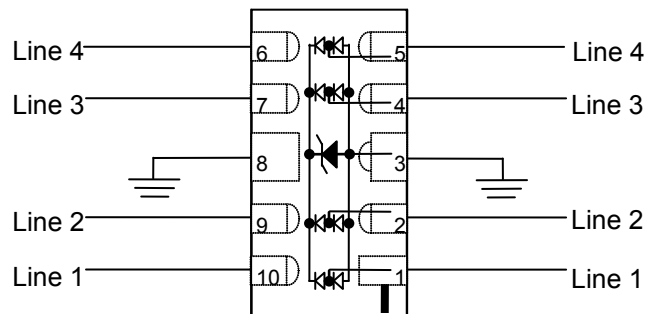
Applications Information

The UMD0524P is designed for have ease of PCB layout by allowing the traces to run straight through the device. The PCB traces can be used to connect the pin pairs for each line. For example line 1 enters at Pin 1 and exits at Pin 10 and the PCB trace connects Pin 1 and 10 together. Ground is connected at pins 3 and 8. Note that one large ground pad should be used in lieu of two separate pads.

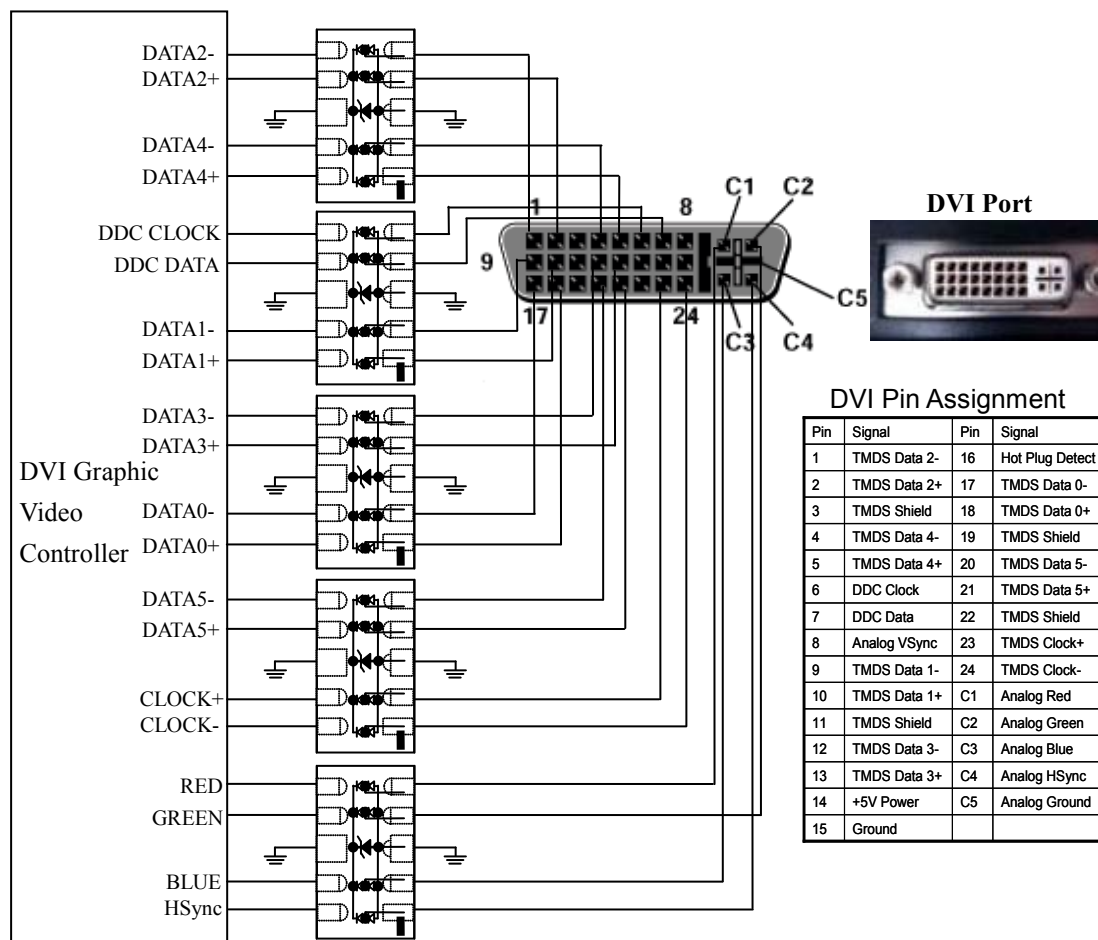
Flow through layout protection

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1 and 10
- Line 2 is connected to Pin 2 and 9
- Line 3 is connected to Pin 4 and 7
- Line 4 is connected to Pin 5 and 6
- Pin 3 and 8 are connected to Ground

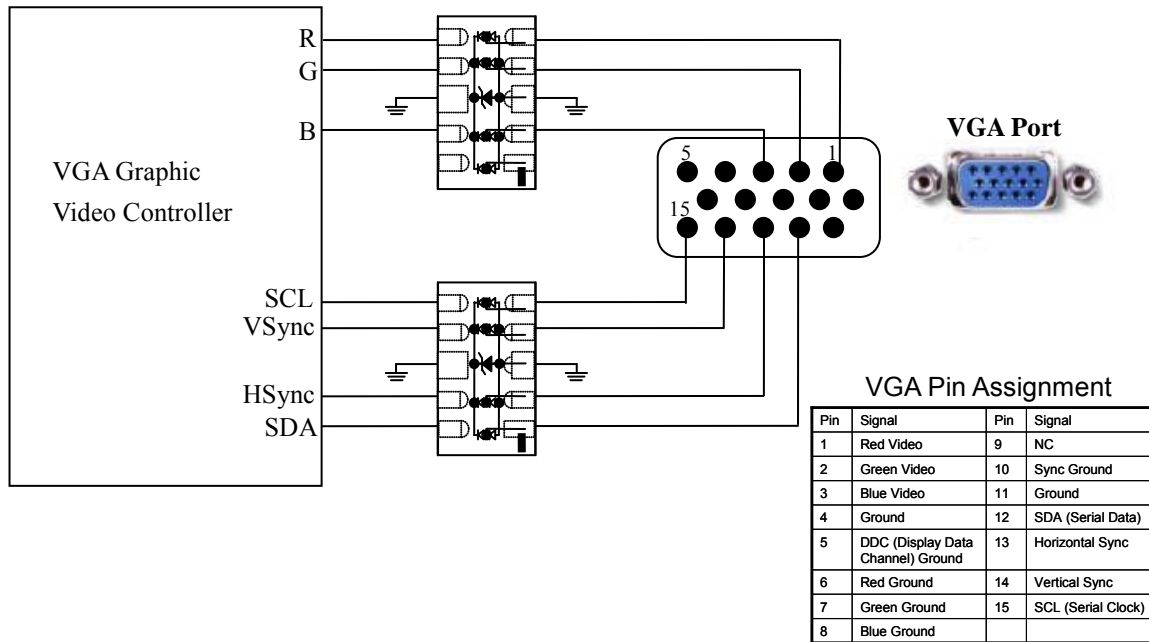


UMD0524P on DVI Port App

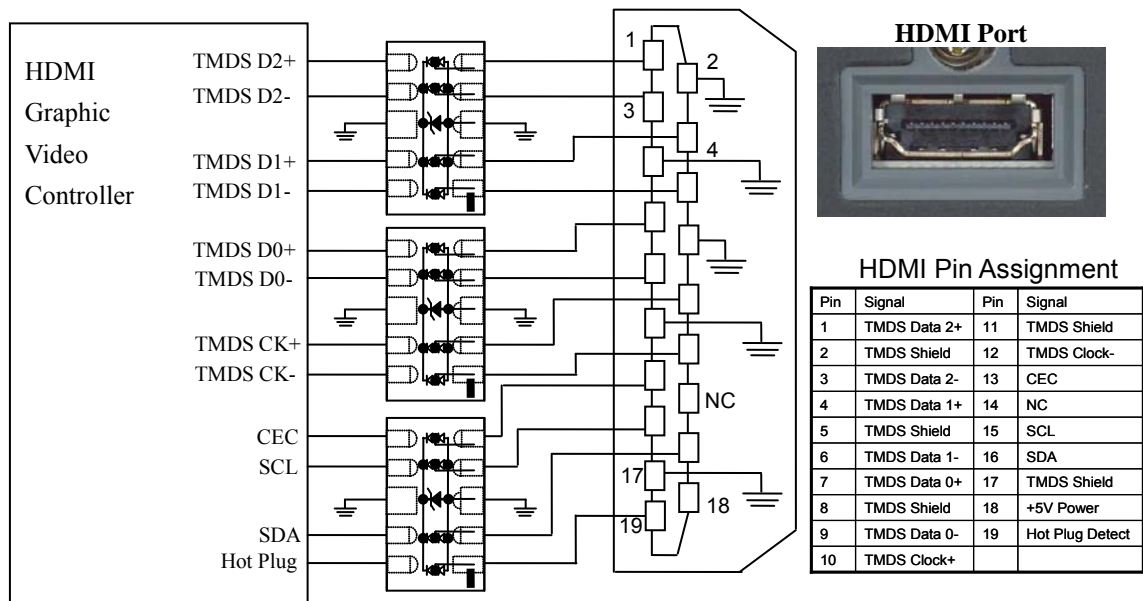


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMD0524P on VGA Port Application

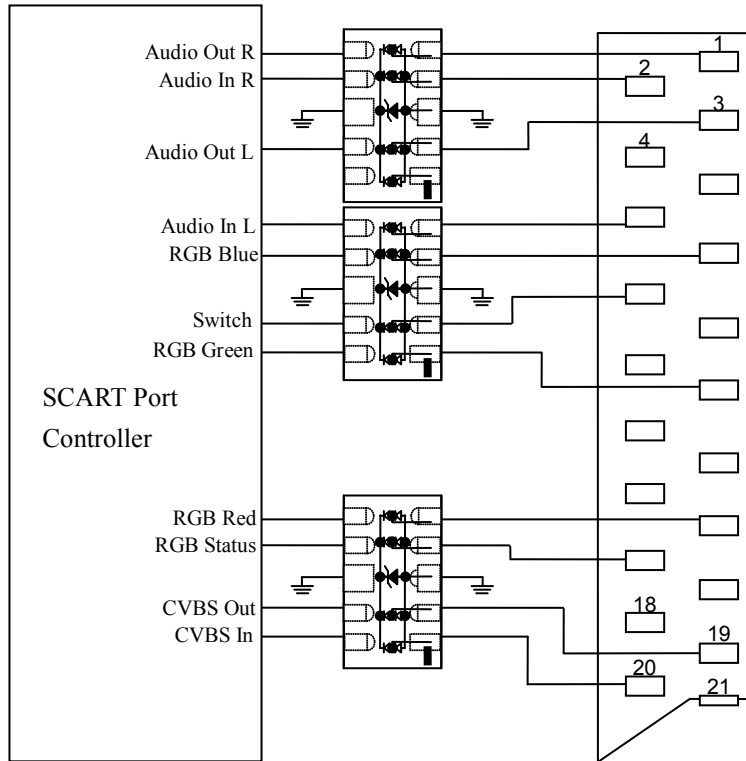


UMD0524P on HDMI Port Application



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

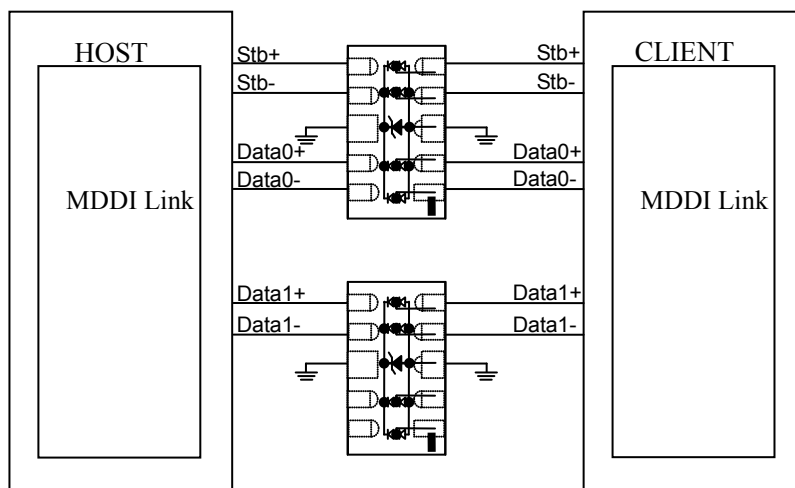
UMD0524P on Scart Port Application



Scart Pin Assignment

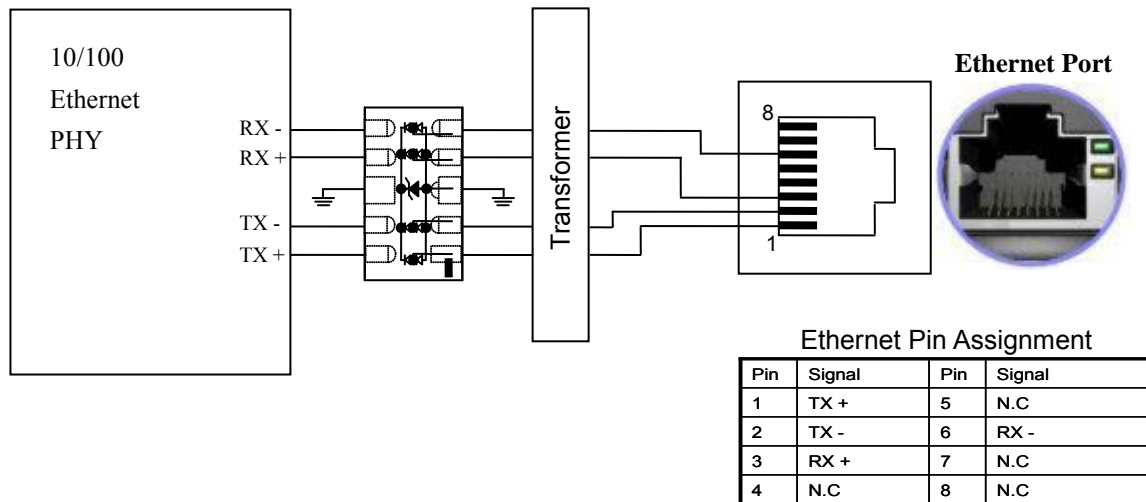
Pin	Signal	Pin	Signal
1	Audio Out R	12	N.C
2	Audio In R	13	Red Gnd
3	Audio Out L	14	RGB Status Gnd
4	Audio Gnd	15	RGB Red
5	Blue Gnd	16	RGB Status
6	Audio in L	17	CVBS Out Gnd
7	RGB Blue	18	CVBS In Gnd
8	Switch	19	CVBS Out
9	Green Gnd	20	CVBS In
10	N.C	21	Gnd
11	RGB Green		

UMD0524P on MDDI (Type 2) Application

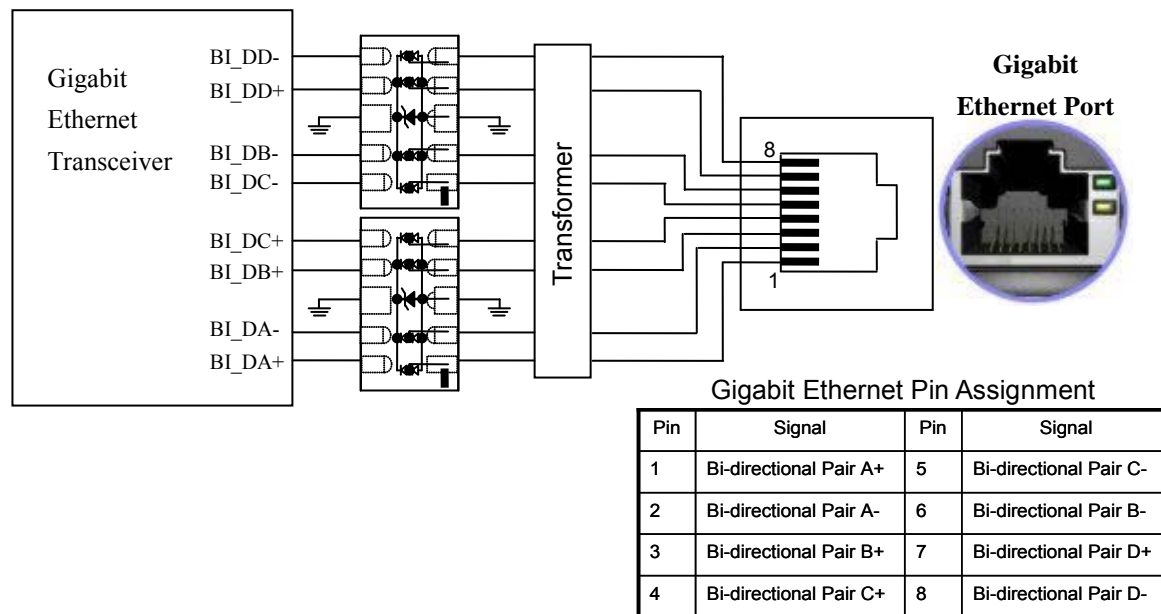


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

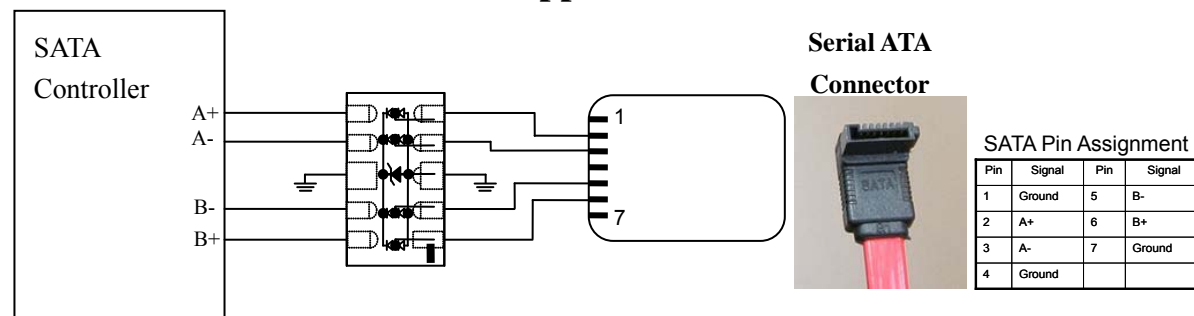
UMD0524P on 10/100 Base Ethernet Port Application



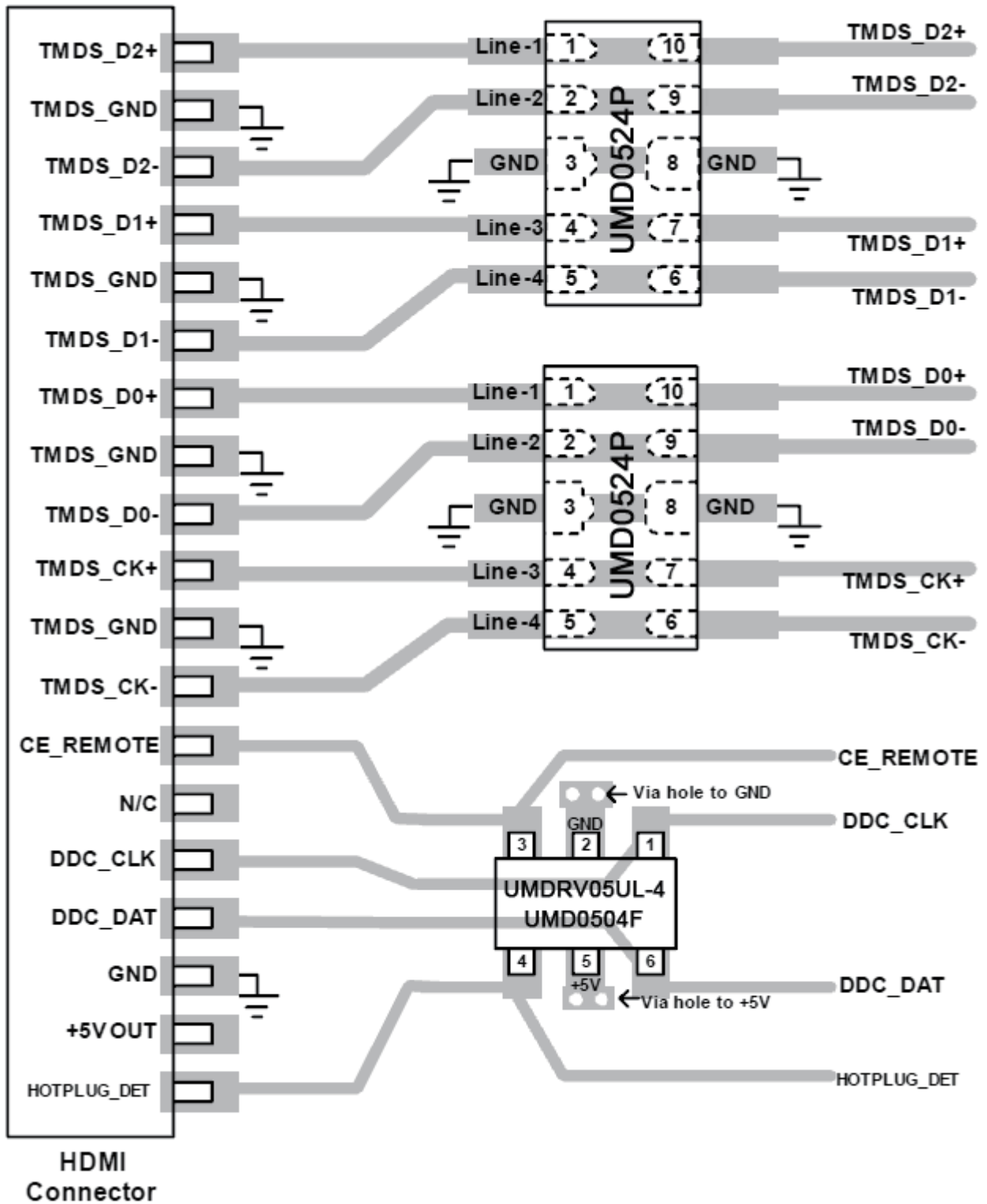
UMD0524P on Gigabit Ethernet Port Application



UMD0524P on Serial ATA Port Application



HDMI Protection for High and Low speed signals



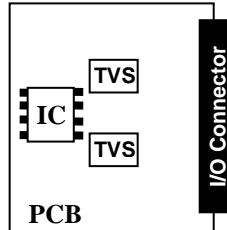
4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Circuit Board Layout Recommendations

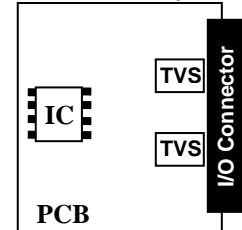
Good circuit board layout is critical for creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

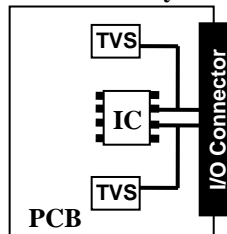
Poor PCB Layout



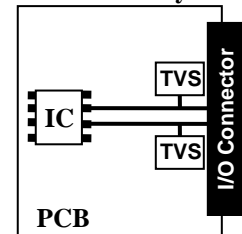
Good PCB Layout



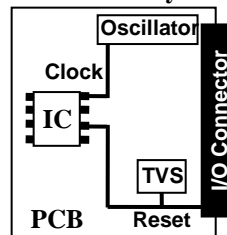
Poor PCB Layout



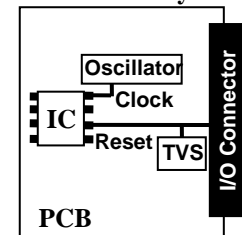
Good PCB Layout



Poor PCB Layout



Good PCB Layout

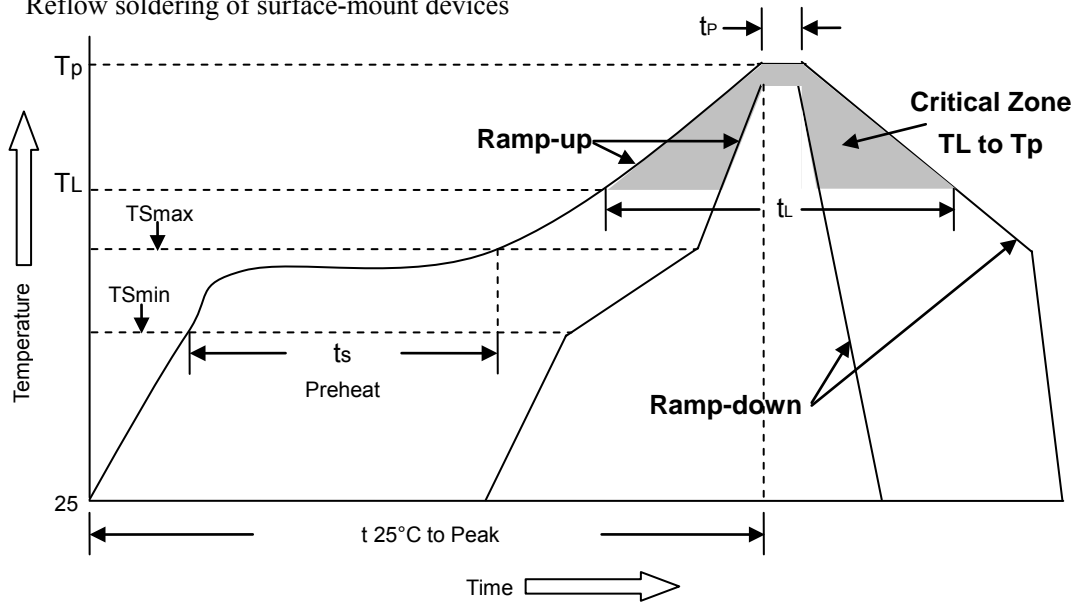


Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection
Soldering Method for UMD's Products

1. Storage environment: Temperature = 10°C~35°C Humidity = 65%±15%
2. Reflow soldering of surface-mount devices



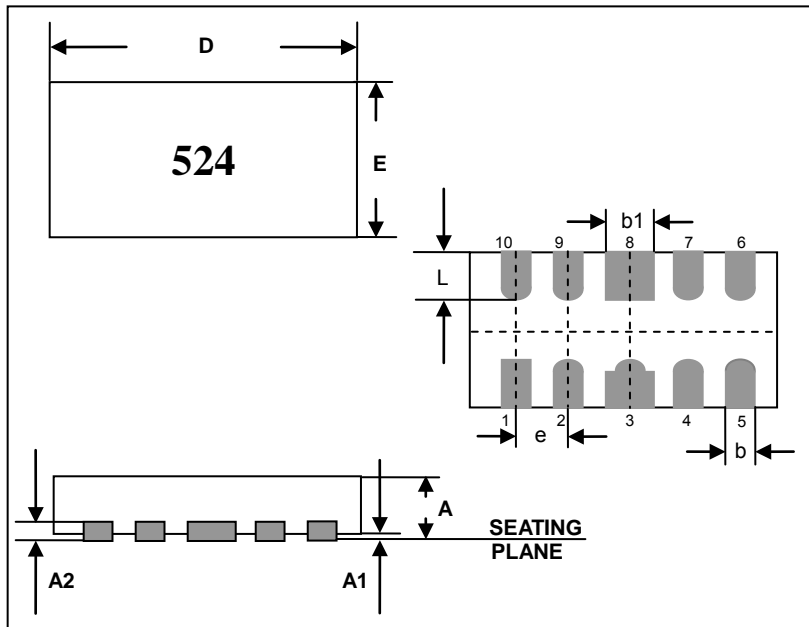
Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec
Preheat	
- Temperature Min (T _{Smin})	150°C
- Temperature Max (T _{Smax})	200°C
- Time (min to max) (t _s)	60~180sec
T _{Smax} to TL	
- Ramp-up Rate	<3°C/sec
Time maintained above:	
- Temperature (TL)	220°C
- Time (t _L)	50~145sec
Peak Temperature (T _P)	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t _p)	20~40sec
Ramp-down Rate	<6°C/sec
Time 25°C to peak Temperature	<8 minutes

Flow (wave) soldering (solder dipping)

Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec

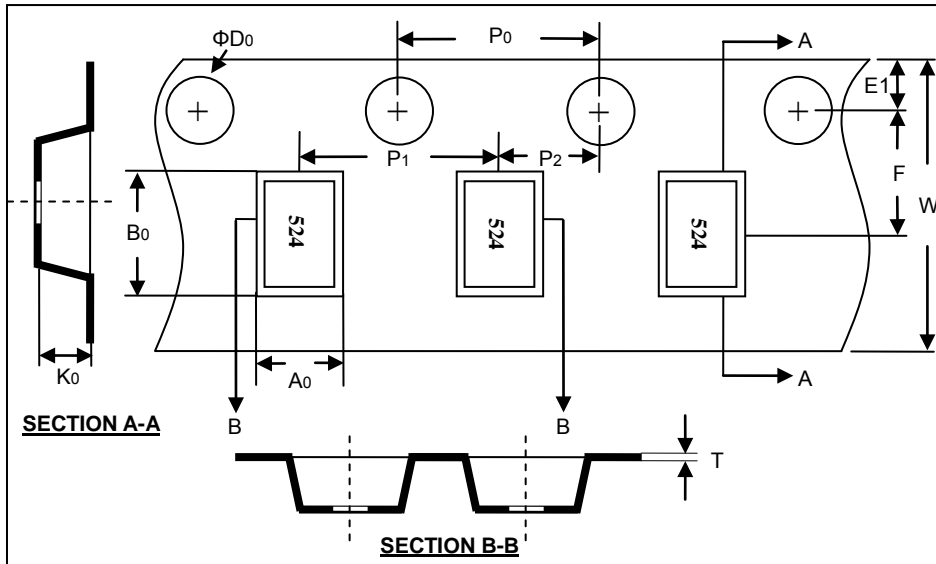
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DFN-10 Dimension Drawing

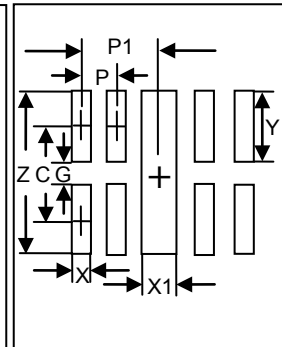


Dim	Dimensions			
	Inches		mm	
	Min	Max	Min	Max
A	0.020	0.026	0.50	0.65
A1	0.000	0.002	0.00	0.05
A2	0.005		0.13	
b	0.006	0.010	0.15	0.25
b1	0.014	0.018	0.35	0.45
D	0.094	0.102	2.40	2.60
E	0.035	0.043	0.90	1.10
e	0.020 BSC		0.50 BSC	
L	0.012	0.017	0.30	0.43

DFN-10 Carrier Dimension



Mounting Pattern



Typical		
Dim	MM	Inches
Z	1.55	0.061
C	0.88	0.035
G	0.20	0.008
Y	0.68	0.027
X	0.20	0.008
X1	0.40	0.016
P	0.50	0.020
P1	1.00	0.039

Dimensions in mm.

Reel Dia.	Tape Width	A0	B0	K0	T	D0
178mm (7")	8mm	1.23±0.05	2.70±0.05	0.70±0.05	0.35±0.05	1.50±0.10
P0	P1	P2	E1	F	W	
4.00±0.10	4.00±0.10	2.00±0.05	1.75±0.10	3.50±0.05	8.00±0.30	



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Marking Code

Part Number	Device Marking
UMD0524P	524

Ordering Information

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMD0524P	Pb-Free	3,000	7 inch

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