

**8 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection**
**Description**

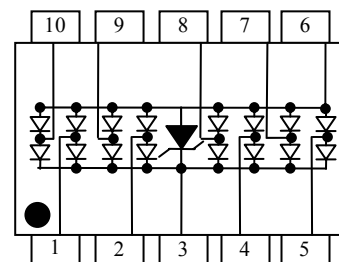
Dual-rail clamp diodes are designed to provide ESD protection for high speed data interfaces. They are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading.

The UMD0508M consists of eight pairs of diodes in series which steer the positive or negative ESD current pulse to either the positive ( $V_p$ ) or negative ( $V_n$ ) supply rail, and a TVS diode which is embedded between  $V_p$  and  $V_n$ . The low capacitance array configuration allows the user to protect eight high-speed data or transmission lines. The TVS diode prevents over-voltage on the power line, protecting any down stream components.

**Features**

- \* Dual-Rail Clamp technology
- \* MSOP-10 package
- \* Bi-Directional protection
- \* Protects eight data lines and one power line
- \* Low channel input capacitance of 0.8pF typical
- \* Working voltage: 5V
- \* Low clamping factor  $V_{cl}/V_{br}$
- \* Low leakage current
- \* Full RoHS compliance
- \* Complies with the following standards:
  - IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
  - IEC 61000-4-4 (EFT) (5/50ns)
  - IEC 61000-4-5 (Surge) (8/20 $\mu$ s)

**Ultra Low Capacitance Series TVS**

**MSOP-10 Pin Configuration**


<u>Pin</u>	<u>Description</u>
1,2,4,5,7,8,9 and 10	I/O
6	$V_n$
3	$V_p$

**Mechanical Characteristics**

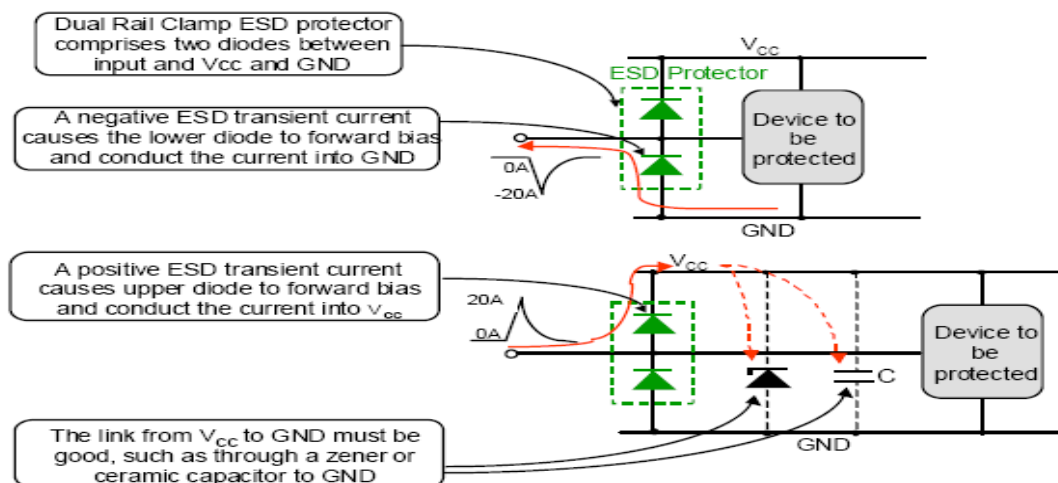
- \* Molded JEDEC MSOP-10 package
- \* Weight 30 milligrams (Approximate)
- \* Available in Lead-Free Pure-Tin Plating
- \* Solder Reflow Temp.: Pure-Tin (Sn), 260-270°C
- \* Consult Factory for Leaded Device Availability
- \* Flammability Rating UL 94V-0
- \* 12mm Tape and Reel per EIA Standard 481
- \* Device Marking: Marking Code,  
Pin one defined by DOT

**Applications**

- \* HDMI and DVI Port Protection
- \* 10/100/1000 Ethernet Port Protection
- \* USB2.0 Power and Data Line Protection
- \* IEEE1394 Firewire Port Protection
- \* Set Top Boxes and Digital TV
- \* Compact Flash Card

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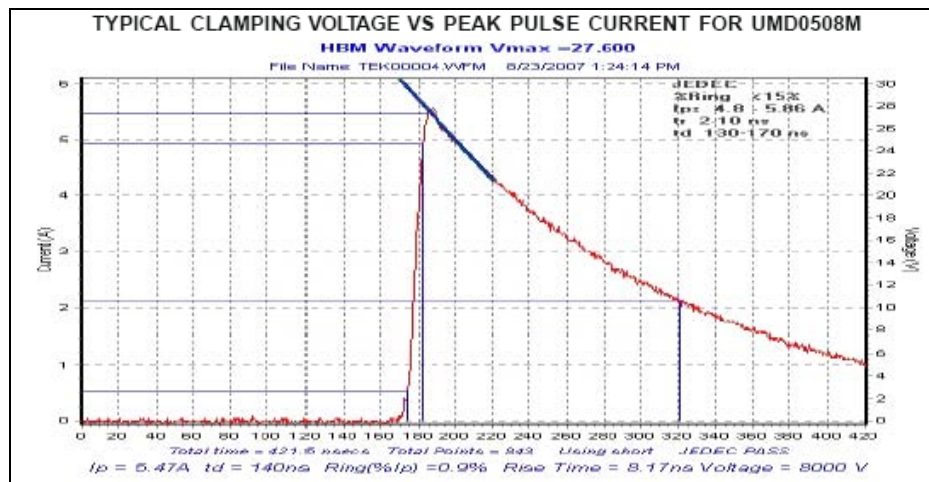
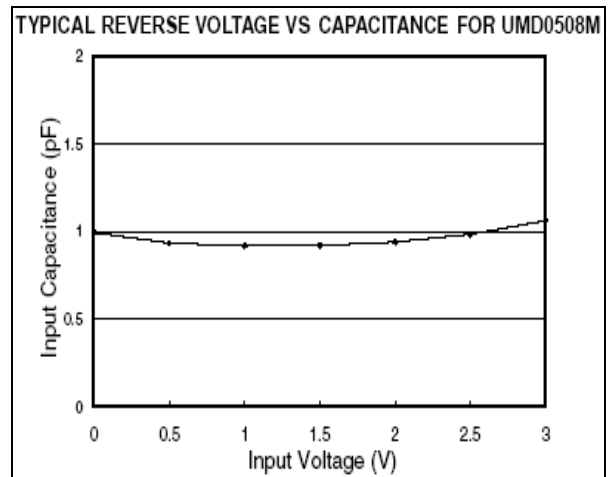
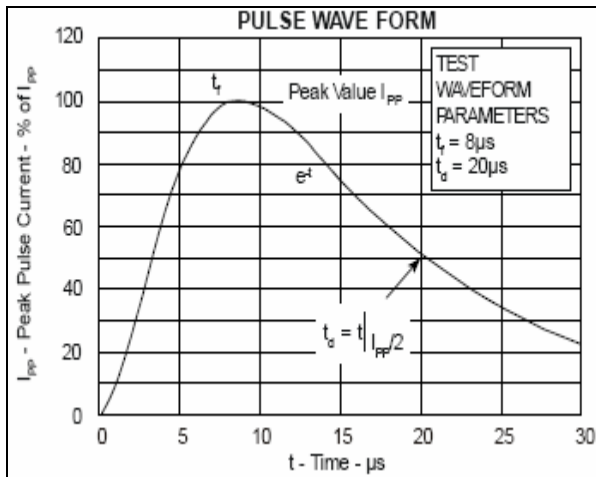
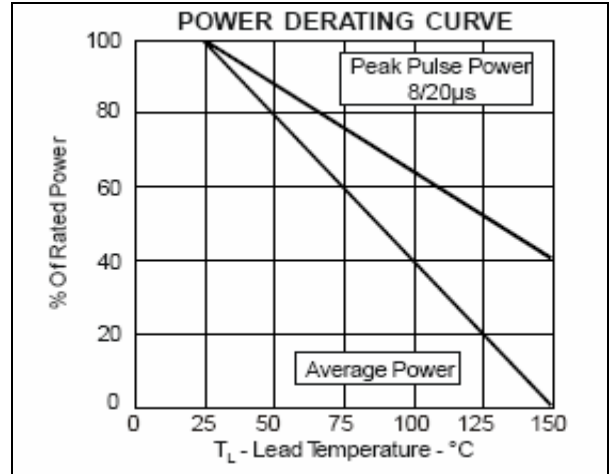
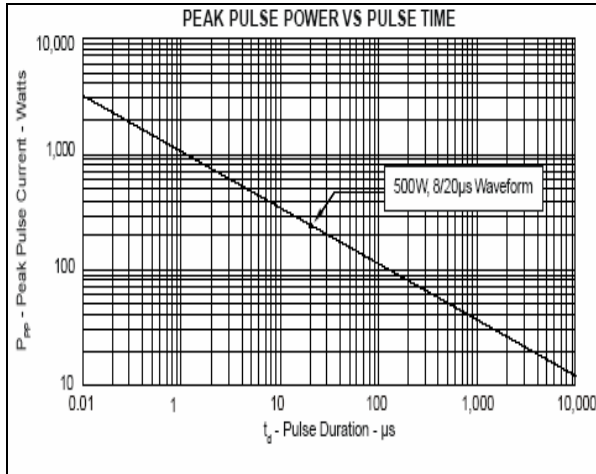
<b>Absolute Maximum Ratings @ 25°C unless otherwise specified</b>			
Parameter	Symbol	Value	Units
Peak Pulse Power; pulse waveform = 8/20µs	P <sub>pp</sub>	200	W
Peak Pulse Current; pulse waveform = 8/20µs	I <sub>pp</sub>	5.4	A
ESD per IEC 61000-4-2 (Air)	V <sub>pp</sub>	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature	T <sub>j</sub>	-77 to 347	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

**Dual-Rail Clamp Diode Protection**


<b>Electrical Characteristics @ 25°C unless otherwise specified</b>					
Parameter	Conditions	Minimum	Typical	Maximum	Units
Operating Supply Voltage (V <sub>p</sub> )			3.3	5.5	V
Operating Supply Current (I <sub>p</sub> )	V <sub>p</sub> =3.3v			8	µA
Diode Forward Voltage	I <sub>f</sub> =8mA				
Top Diode		0.6	0.8	0.95	V
Bottom Diode		0.6	0.8	0.95	V
Leakage Current	V <sub>p</sub> =5v		±0.1	±1	µA
Signal Clamp Voltage	I <sub>pp</sub> =10mA	6.5	7.5	9.0	V
Clamping Voltage +ve Transient	I <sub>pp</sub> =1A, T <sub>p</sub> =8/20µs		9		V
-ve Transient			-1.5		V
Input Capacitance @1MHz	V <sub>p</sub> =3.3v, V <sub>i/o</sub> =1.65v	0.6	0.8	1.0	pF

8 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Electrical Characteristics Graphs



**8 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection**

**Applications Information**

To protect data lines and the power line.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 2
- Pin 3 is connected to Vp
- Line 3 is connected to Pin 4
- Line 4 is connected to Pin 5
- Pin 6 is connected to ground
- Line 5 is connected to Pin 7
- Line 6 is connected to Pin 8
- Line 7 is connected to Pin 9
- Line 8 is connected to Pin 10

Isolation from the power supply.

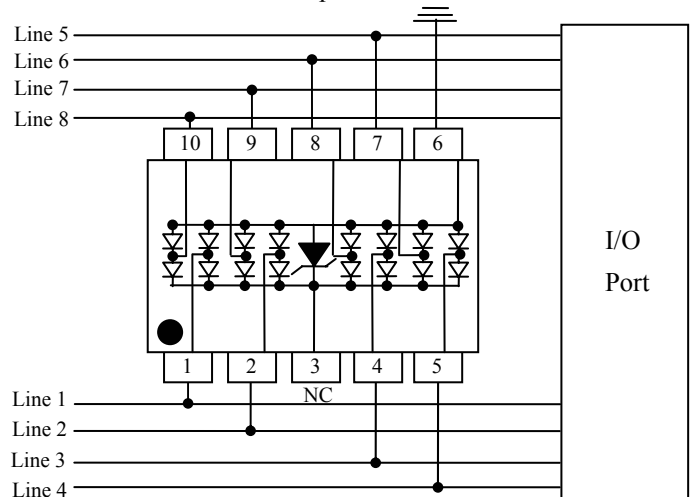
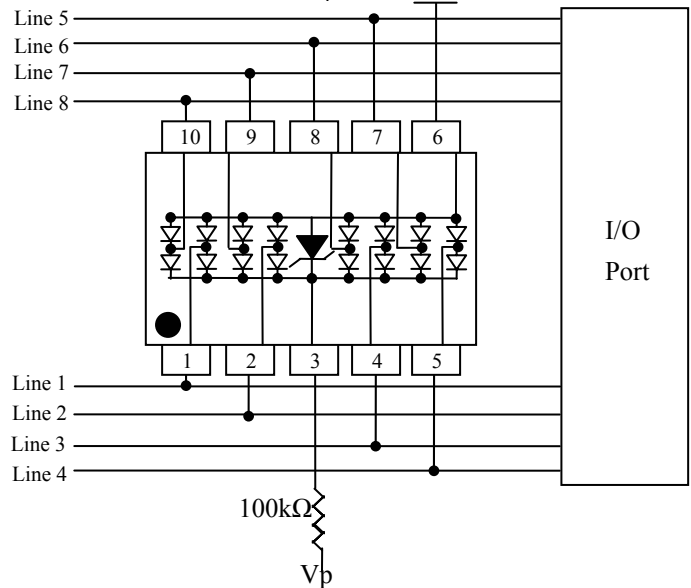
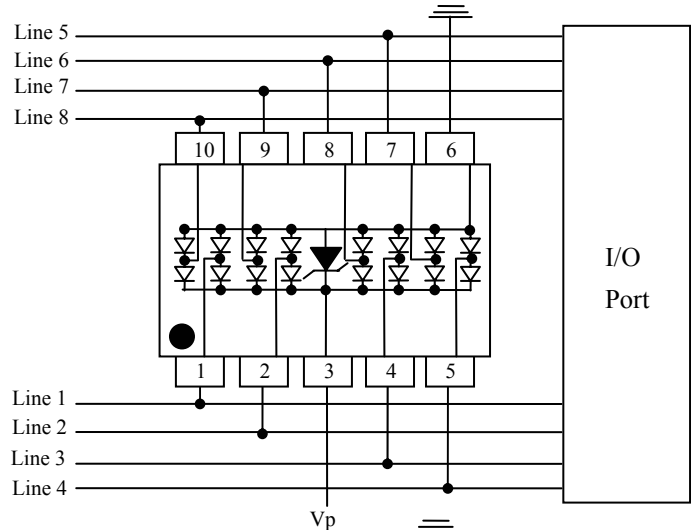
Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 2
- Pin 3 is connected to series resistor
- Line 3 is connected to Pin 4
- Line 4 is connected to Pin 5
- Pin 6 is connected to ground
- Line 5 is connected to Pin 7
- Line 6 is connected to Pin 8
- Line 7 is connected to Pin 9
- Line 8 is connected to Pin 10

No positive supply reference is available.

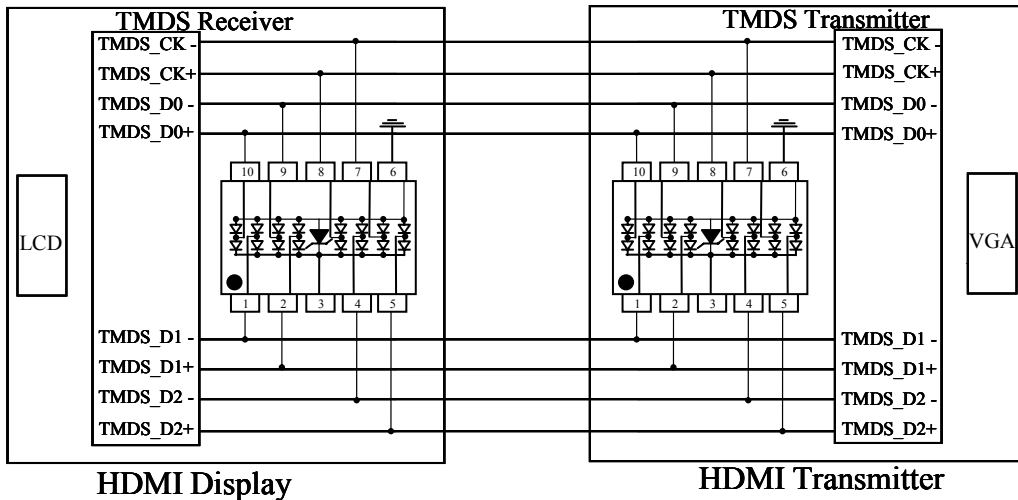
Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 2
- Pin 3 is not connected
- Line 3 is connected to Pin 4
- Line 4 is connected to Pin 5
- Pin 6 is connected to ground
- Line 5 is connected to Pin 7
- Line 6 is connected to Pin 8
- Line 7 is connected to Pin 9
- Line 8 is connected to Pin 10



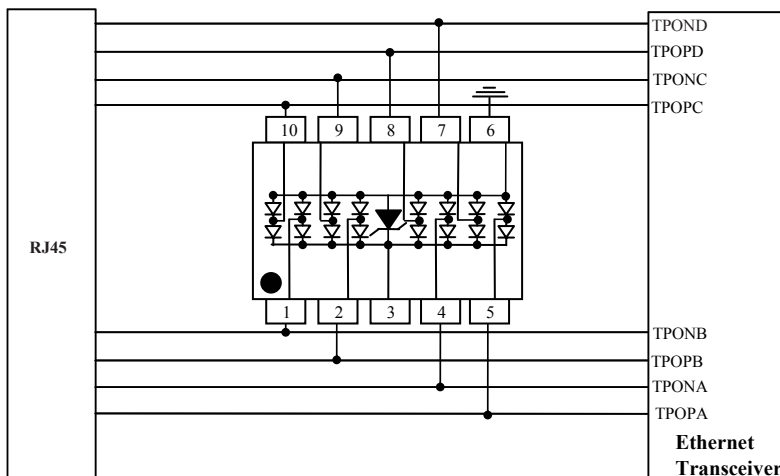
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UMD0508M on HDMI Port Application



HDMI ports have become standard features on today’s consumer electronics devices, such as digital TVs, DVD recorders, and set top boxes. The small geometry of a HDMI graphic chip will make it more susceptible to ESD and cable discharge events. The high-speed transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the IC. The UMD0508M offers full protection against ESD and its low capacitance of 0.8pF, ensures signal integrity.

UMD0508M on 10/100/1000 Ethernet Port Application

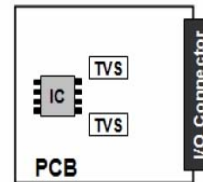
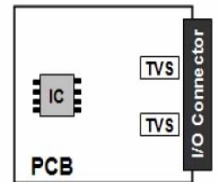
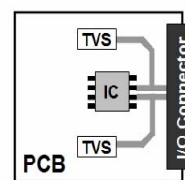
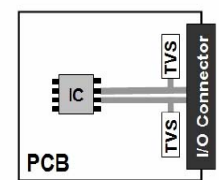
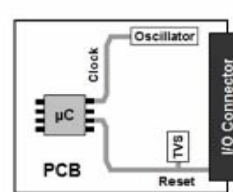
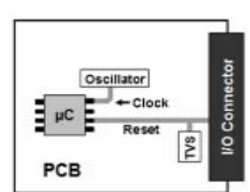


Ethernet ICs are vulnerable to damage from electro static discharge (ESD), lightning, and cable discharge events (CDE). The internal protection in the PHY chip, often is not enough due to the high energy of these disturbances. The fatal discharge can occur differentially across the transmit or receive line pair or between any line and ground (common mode). Common mode and differential mode protection against ESD and CDE discharges can be achieved by connecting the UMD0508M on the PHY side of the Ethernet circuit.

**8 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection**
**Circuit Board Layout Recommendations**

Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

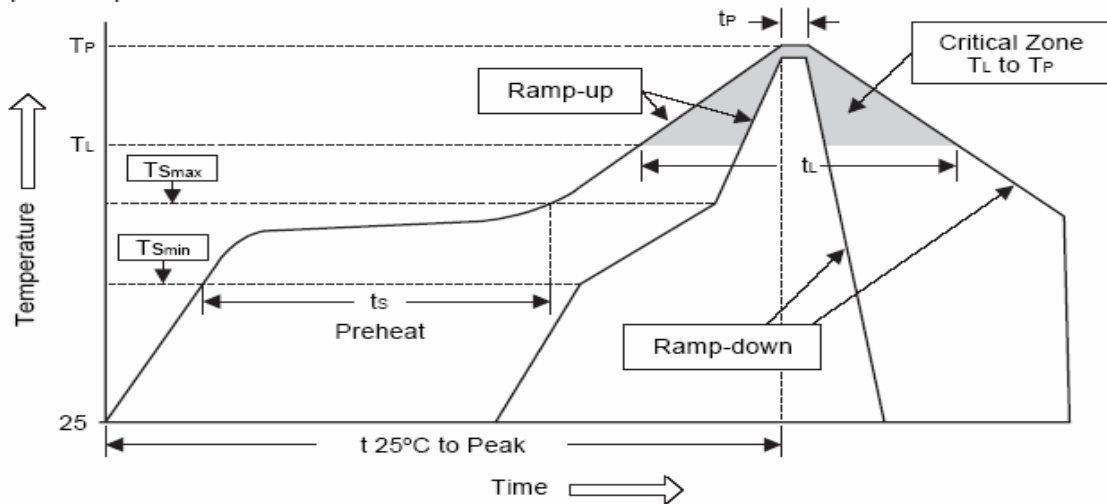
**Poor PCB Layout**

**Good PCB Layout**

**Poor PCB Layout**

**Good PCB Layout**

**Poor PCB Layout**

**Good PCB Layout**

**Matte Tin Lead Finish**

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

**8 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection**
**Soldering Method for UMD's Products**

1. Storage environment: Temperature = 10°C~35°C Humidity = 65%±15%
2. Reflow soldering of surface-mount devices

Temperature profile



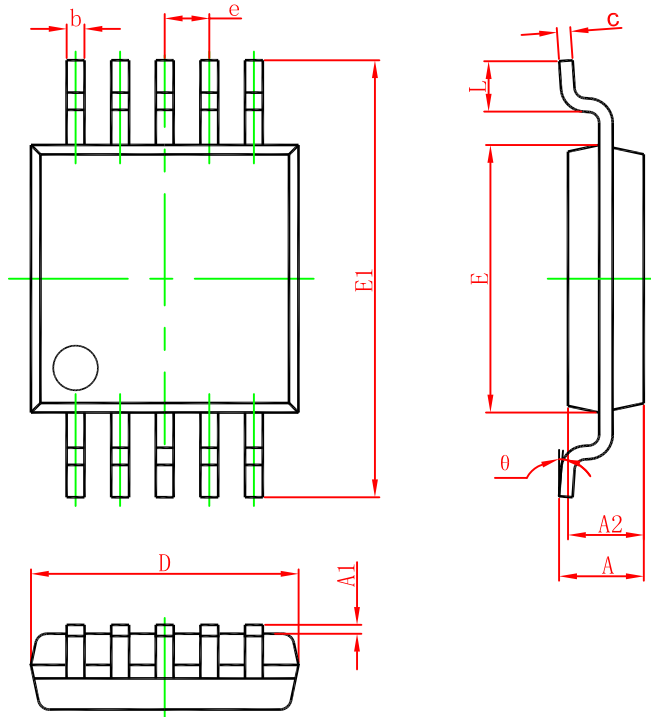
Profile Feature	Pb-Free Assembly
Average ramp-up rate (T <sub>L</sub> to T <sub>P</sub> )	<3°C/sec
Preheat	
- Temperature Min (T <sub>Smin</sub> )	150°C
- Temperature Max (T <sub>Smax</sub> )	200°C
- Time (min to max) (t <sub>s</sub> )	60~180sec
T <sub>Smax</sub> to T <sub>L</sub>	
- Ramp-up Rate	<3°C/sec
Time maintained above:	
- Temperature (T <sub>L</sub> )	220°C
- Time (t <sub>L</sub> )	50~145sec
Peak Temperature (T <sub>P</sub> )	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t <sub>P</sub> )	20~40sec
Ramp-down Rate	<6°C/sec
Time 25°C to peak Temperature	<8 minutes

Flow (wave) soldering (solder dipping)

Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec

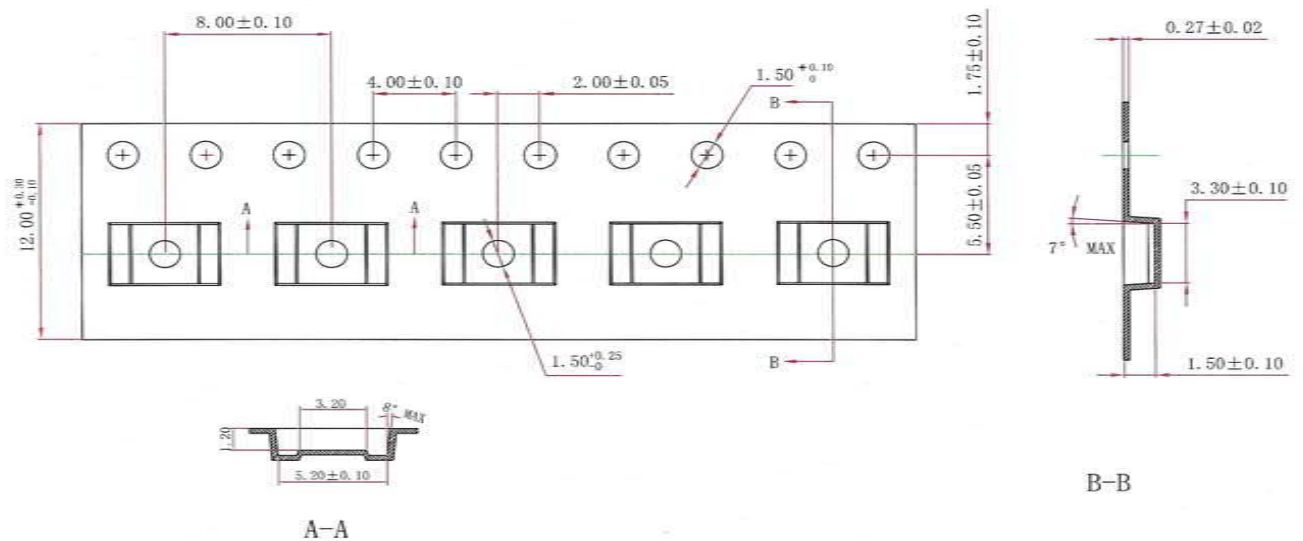
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MSOP-10 Dimension Drawing



Symbol	Dimensions In Millimeters		Dimensions In Inchs	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

MSOP-10 Carrier Dimension





**8 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection**

**Marking Code**

Part Number	Device Marking
UMD0508M	A8MR

**Ordering Information**

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMD0508M	Pb-Free	6,000	35 inch

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