

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection
Description

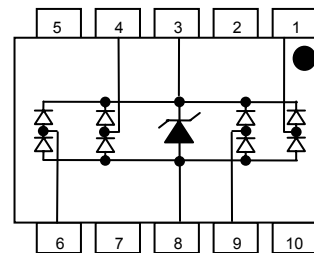
Dual-rail clamp diodes are designed to provide ESD protection for high speed data interfaces. They are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading.

The UMD0504M consists of four pairs of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_p) or negative (V_n) supply rail, and a TVS diode which is embedded between V_p and V_n . The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The TVS diode prevents over-voltage on the power line, protecting any down stream components.

Features

- * Dual-Rail Clamp technology
- * MSOP-10 package
- * Bi-Directional protection
- * Protects four data lines and one power line
- * Low channel input capacitance of 3.0pF typical
- * Working voltage: 5V
- * Low clamping factor V_{cl}/V_{br}
- * Low leakage current
- * Full RoHS compliance
- * Complies with the following standards:
 - IEC 61000-4-2 (ESD) Air-15kv, Contact-8kv
 - IEC 61000-4-4 (EFT) (5/50ns)
 - IEC 61000-4-5 (Surge) (8/20 μ s)

Low Capacitance Series TVS

MSOP-10 Pin Configuration


<u>Pin</u>	<u>Description</u>
1, 4, 6 and 9	I/O
8	V_n
3	V_p

Mechanical Characteristics

- * Molded JEDEC MSOP-10 package
- * Weight 30 milligrams (Approximate)
- * Available in Lead-Free Pure-Tin Plating
- * Solder Reflow Temp: Pure-Tin (Sn), 260-270°C
- * Consult Factory for Leaded Device Availability
- * Flammability Rating UL 94V-0
- * 12mm Tape and Reel per EIA Standard 481
- * Device Marking: Marking Code,
Pin one defined by DOT

Applications

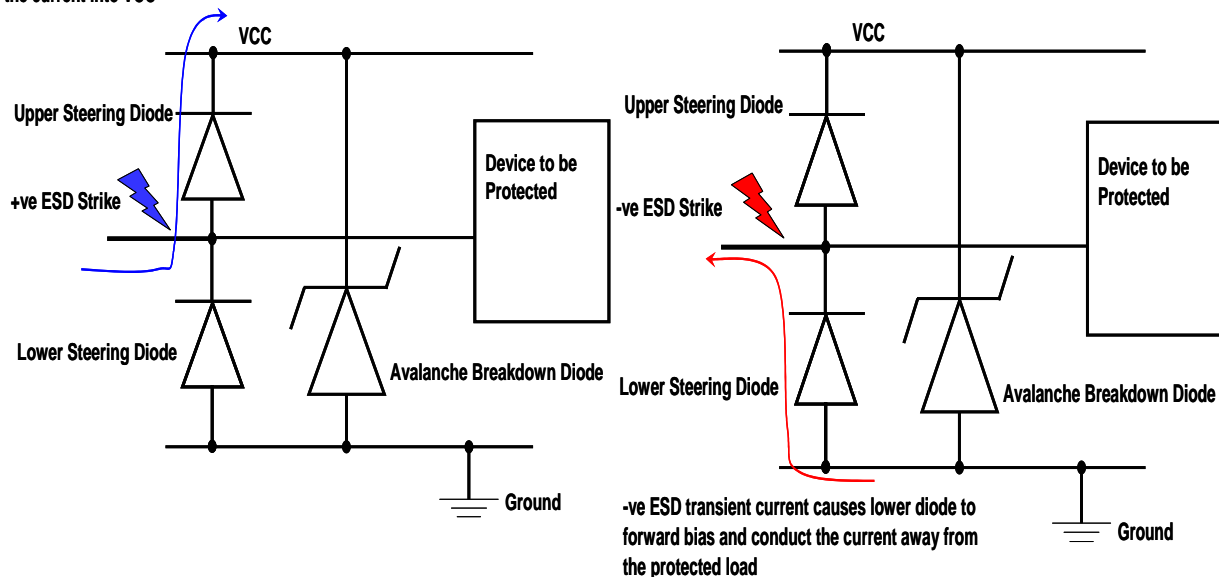
- * HDMI and DVI Port Protection
- * VGA and SCART Port Protection
- * 10/100/1000 Ethernet Port Protection
- * USB2.0 Power and Data Line Protection
- * Notebook Computers
- * Set Top Boxes and Digital TV

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection
Absolute Maximum Ratings @ 25°C unless otherwise specified

Parameter	Symbol	Value	Units
Peak Pulse Power; pulse waveform = 8/20µs	P _{pp}	300	W
Peak Pulse Current; pulse waveform = 8/20µs	I _{pp}	12	A
ESD per IEC 61000-4-2 (Air)	V _{pp}	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature	T _j	-55 to 125	°C
Storage Temperature	T _{stg}	-55 to 150	°C

Dual-Rail Clamp Diode Protection

+ve ESD transient current causes upper diode to forward bias and conduct the current into VCC

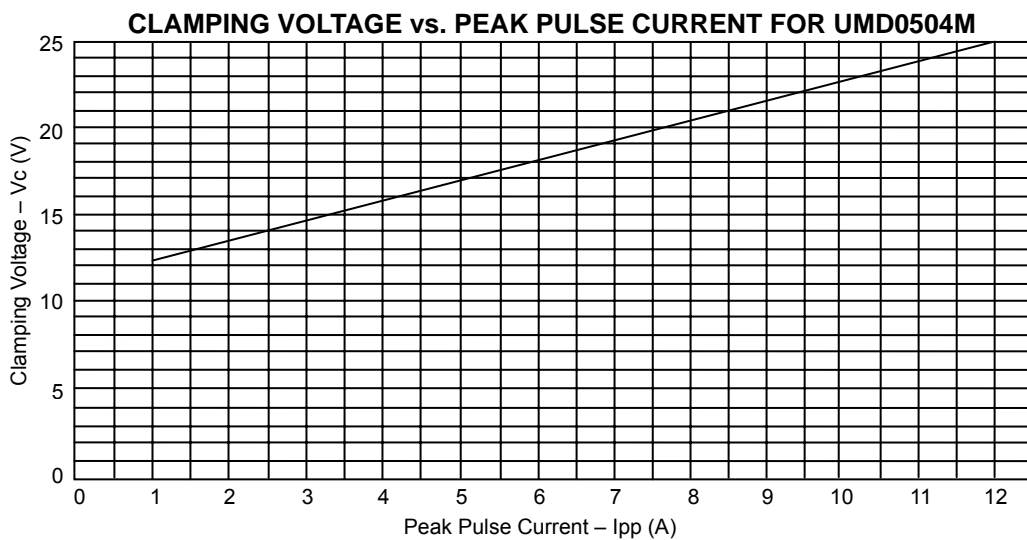
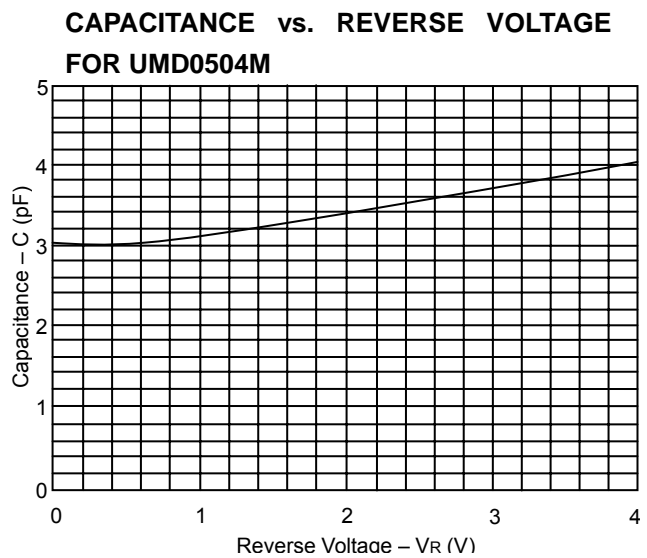
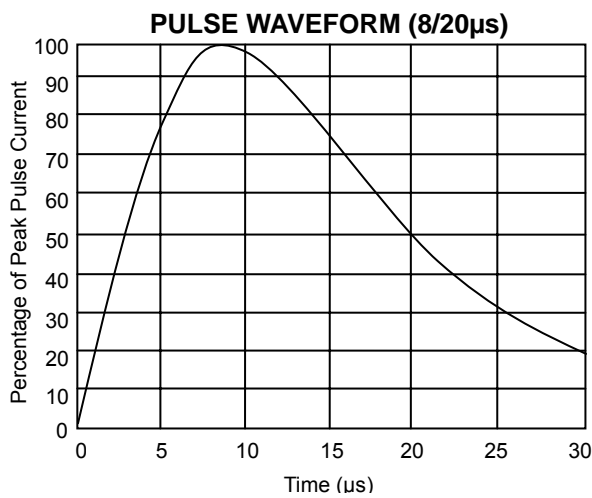
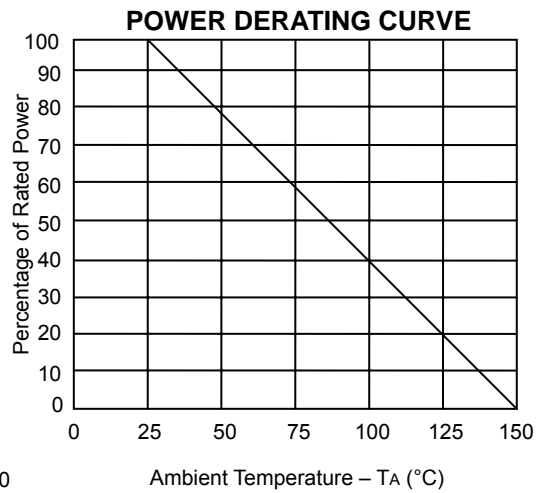
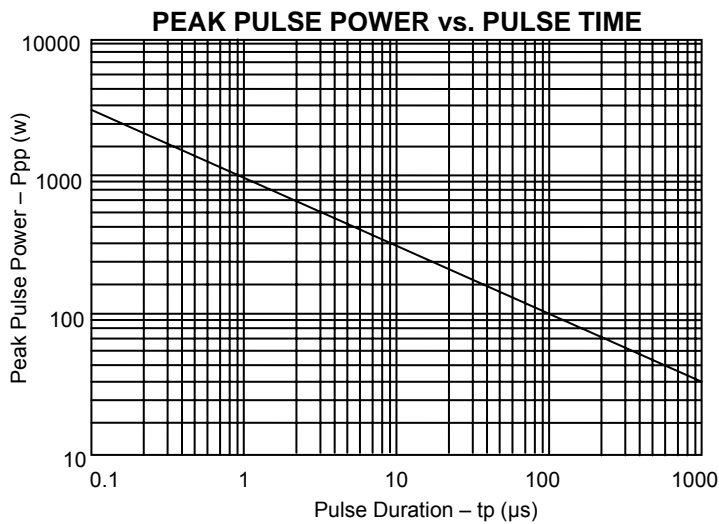

Electrical Characteristics @ 25°C unless otherwise specified

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Stand-off Voltage	V _{wm}	Pin 3 to 8			5.0	V
Breakdown Voltage	V _{br}	I _t =1mA Pin 3 to 8	6.0			V
Leakage Current	I _r	V _{wm} =5V, Pin 3 to 8			5	µA
Forward Voltage	V _f	I _t =15mA			1.2	V
Clamping Voltage	V _c	I _{pp} =1A, T _p =8/20µs			12.5	V
Clamping Voltage	V _c	I _{pp} =12A, T _p =8/20µs			25.0	V
Junction Capacitance	C _j	V _r =0V, f=1MHz I/O to I/O		1.5		
		V _r =0V, f=1MHz I/O to Gnd		3	5	pF



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Electrical Characteristics Graphs



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

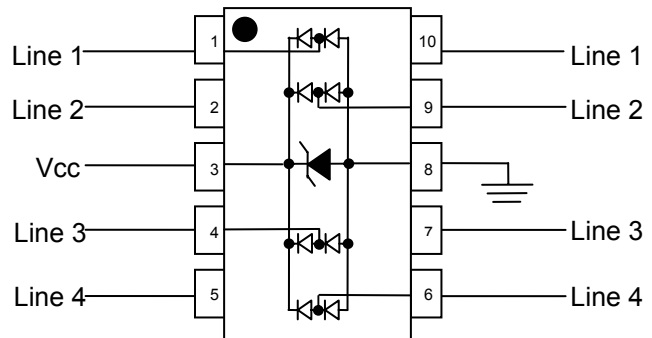
Applications Information

The UMD0504M is designed for have ease of PCB layout by allowing the traces to run straight through the device. The PCB traces can be used to connect the pin pairs for each line.

Flow through layout protection

Circuit connectivity is as follows:

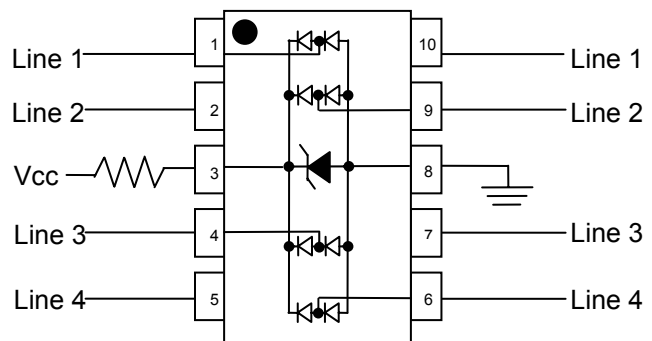
- Line 1 is connected to Pin 1 and 10
- Line 2 is connected to Pin 2 and 9
- Pin 3 is connected to Vcc
- Line 3 is connected to Pin 4 and 7
- Line 4 is connected to Pin 5 and 6
- Pin 8 is connected to Ground



Isolation from the power supply.

Circuit connectivity is as follows:

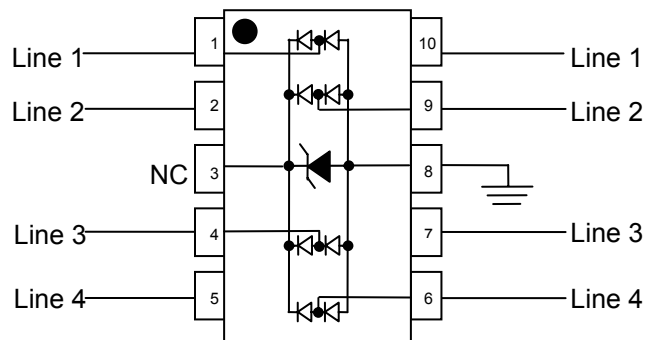
- Line 1 is connected to Pin 1 and 10
- Line 2 is connected to Pin 2 and 9
- Pin 3 is connected to series resistor
- Line 3 is connected to Pin 4 and 7
- Line 4 is connected to Pin 5 and 6
- Pin 8 is connected to Ground



No positive supply reference is available.

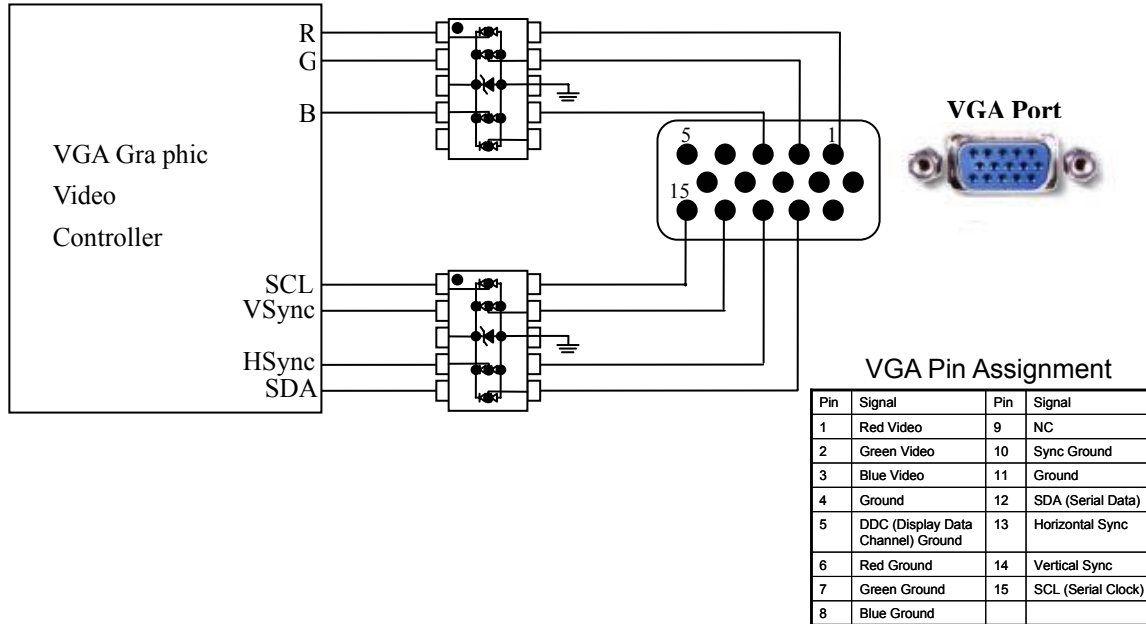
Circuit connectivity is as follows:

- Line 1 is connected to Pin 1 and 10
- Line 2 is connected to Pin 2 and 9
- Pin 3 is not connected
- Line 3 is connected to Pin 4 and 7
- Line 4 is connected to Pin 5 and 6
- Pin 8 is connected to Ground

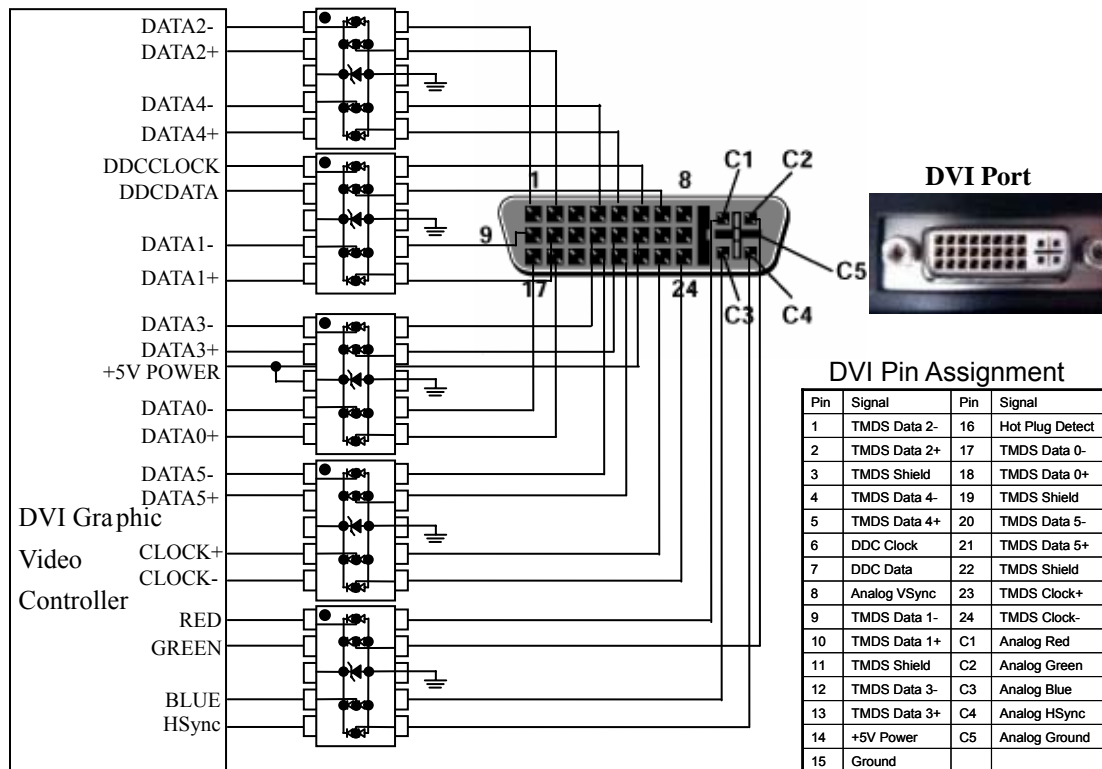


4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMD0504M on VGA Port Application

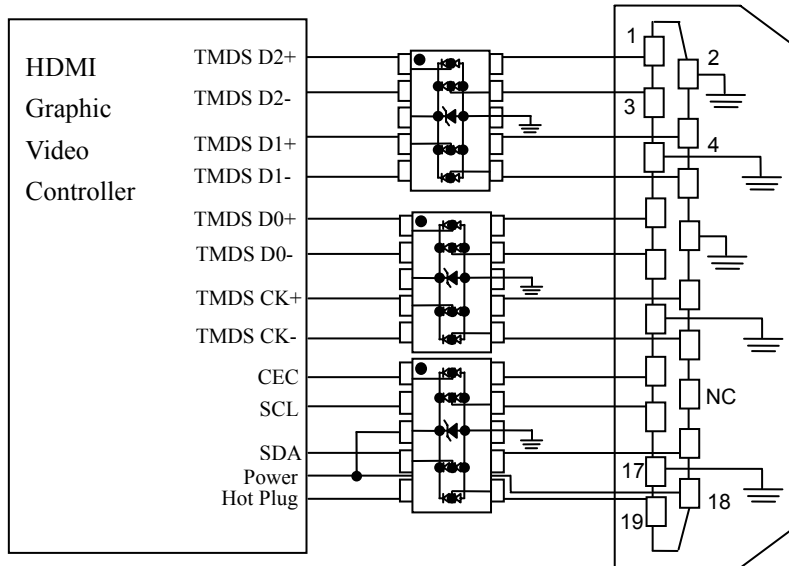


UMD0504M on DVI Port Application



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMD0504M on HDMI Port Application

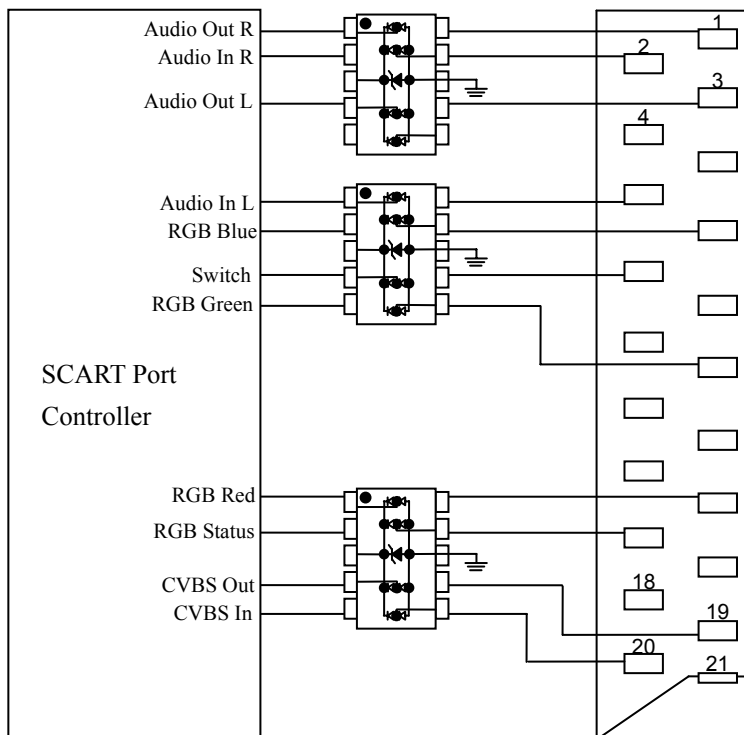


HDMI Port

HDMI Pin Assignment

Pin	Signal	Pin	Signal
1	TMDS Data 2+	11	TMDS Shield
2	TMDS Shield	12	TMDS Clock-
3	TMDS Data 2-	13	CEC
4	TMDS Data 1+	14	NC
5	TMDS Shield	15	SCL
6	TMDS Data 1-	16	SDA
7	TMDS Data 0+	17	TMDS Shield
8	TMDS Shield	18	+5V Power
9	TMDS Data 0-	19	Hot Plug Detect
10	TMDS Clock+		

UMD0504M on Scart Port Application



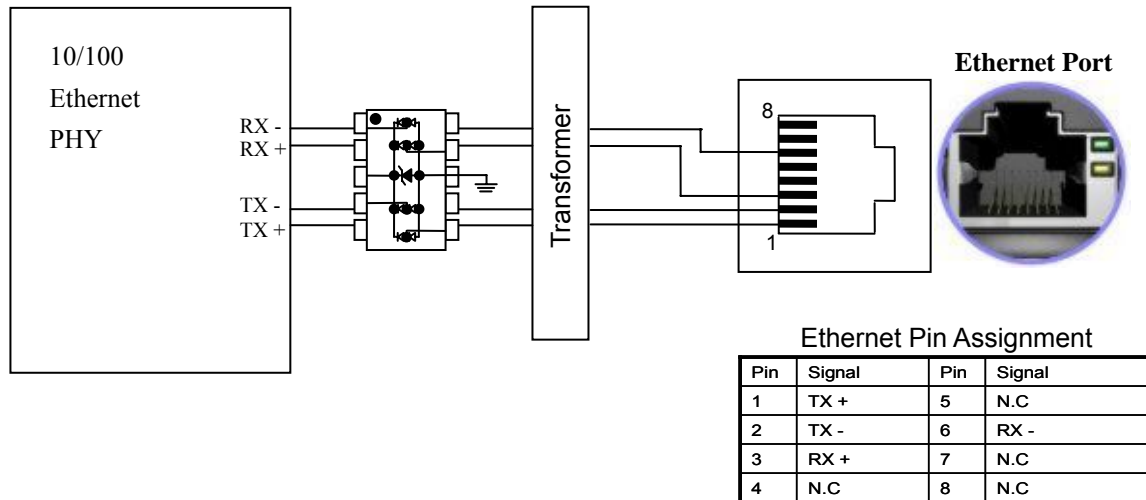
SCART Port

Scart Pin Assignment

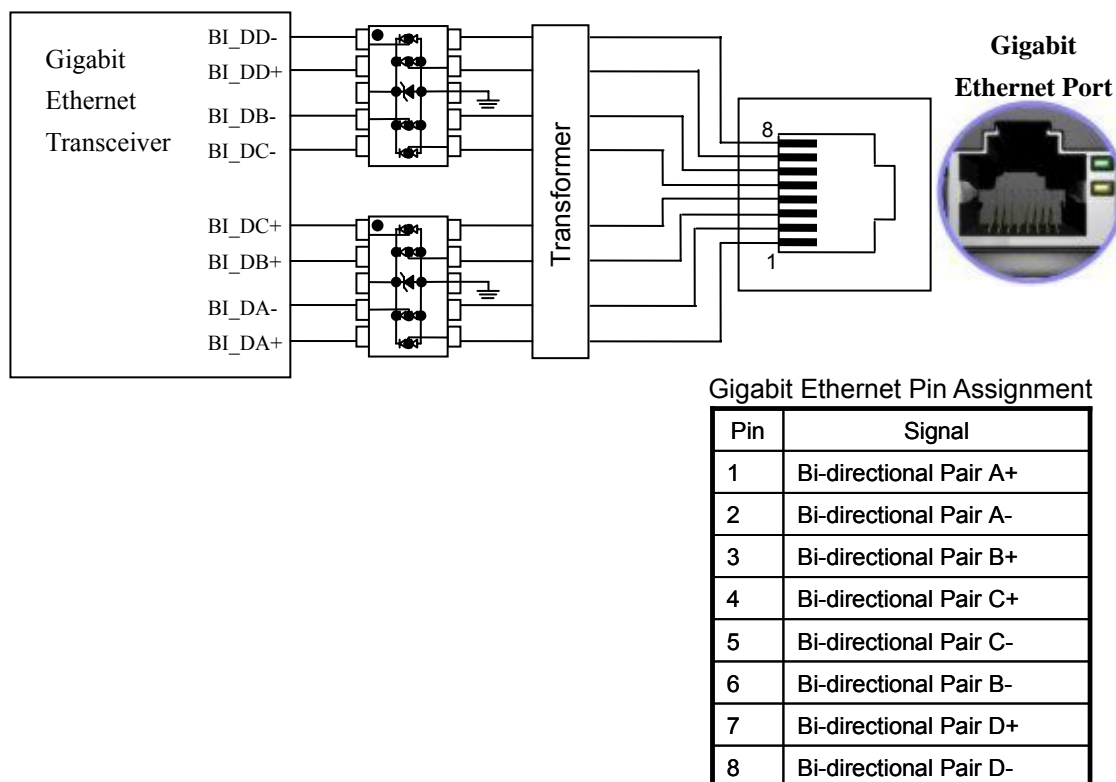
Pin	Signal	Pin	Signal
1	Audio Out R	12	N.C
2	Audio In R	13	Red Gnd
3	Audio Out L	14	RGB Status Gnd
4	Audio Gnd	15	RGB Red
5	Blue Gnd	16	RGB Status
6	Audio in L	17	CVBS Out Gnd
7	RGB Blue	18	CVBS In Gnd
8	Switch	19	CVBS Out
9	Green Gnd	20	CVBS In
10	N.C	21	Gnd
11	RGB Green		

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

UMD0504M on 10/100 Base Ethernet Port Application



UMD0504M on Gigabit Ethernet Port Application



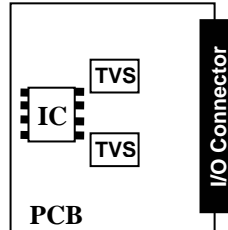
4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Circuit Board Layout Recommendations

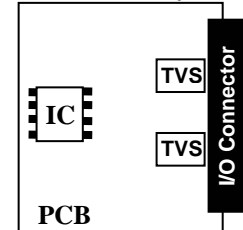
Good circuit board layout is critical for creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- The ESD transient return path to ground should be kept as short as possible.
- Place a TVS and decoupling capacitor between power and ground of components that may be vulnerable to electrostatic discharges to the ground plane.
- Minimize all conductive loops including power and ground loops.
- Use multilayer boards when possible.
- Minimize interconnecting line lengths.
- Never run critical signals near board edges.
- Fill unused portions of the PCB with ground plane.

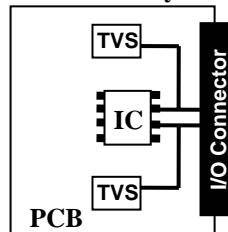
Poor PCB Layout



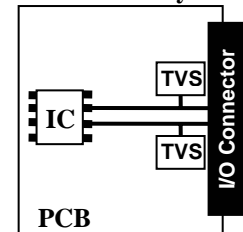
Good PCB Layout



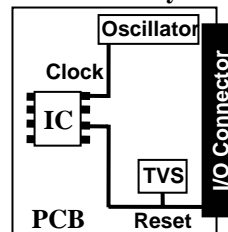
Poor PCB Layout



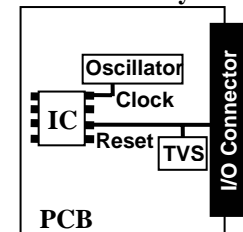
Good PCB Layout



Poor PCB Layout



Good PCB Layout

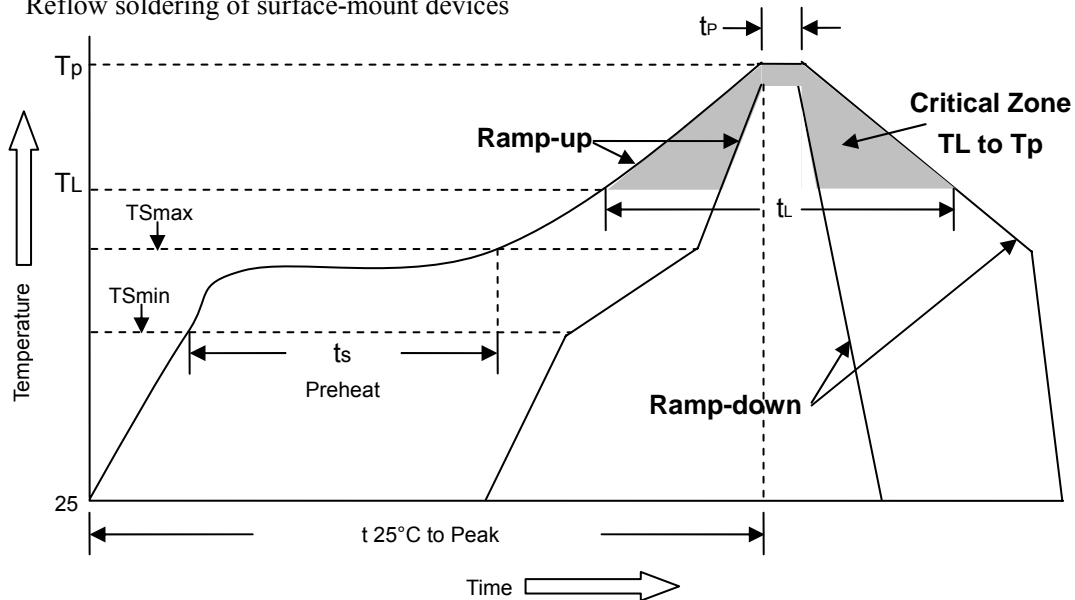


Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. Unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation to solder joint.

4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection
Soldering Method for UMD's Products

1. Storage environment: Temperature = 10°C~35°C Humidity = 65%±15%
2. Reflow soldering of surface-mount devices



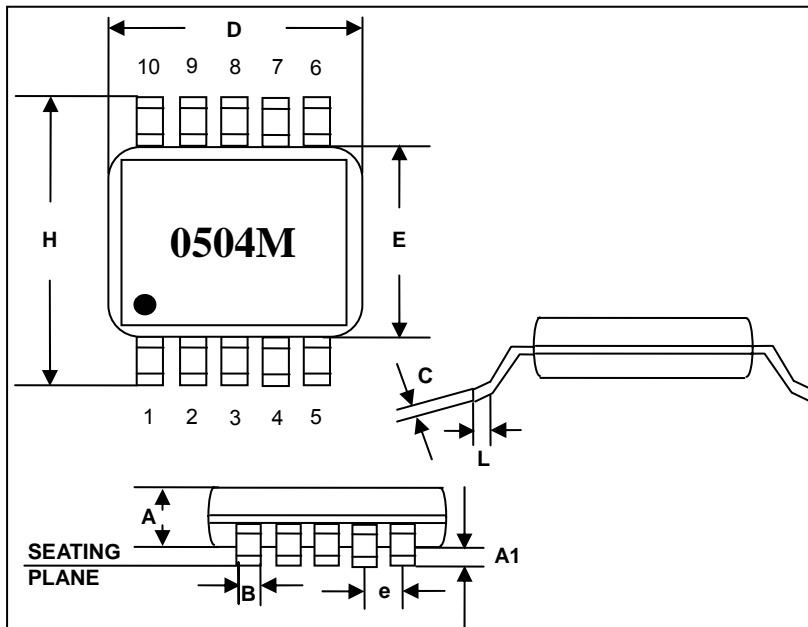
Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec
Preheat	
- Temperature Min (T _{Smin})	150°C
- Temperature Max (T _{Smax})	200°C
- Time (min to max) (t _s)	60~180sec
T _{Smax} to TL	
- Ramp-up Rate	<3°C/sec
Time maintained above:	
- Temperature (TL)	220°C
- Time (t _L)	50~145sec
Peak Temperature (T _P)	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t _p)	20~40sec
Ramp-down Rate	<6°C/sec
Time 25°C to peak Temperature	<8 minutes

Flow (wave) soldering (solder dipping)

Products	Dipping time
Pb devices	5sec±1sec
Pb-Free devices	5sec±1sec

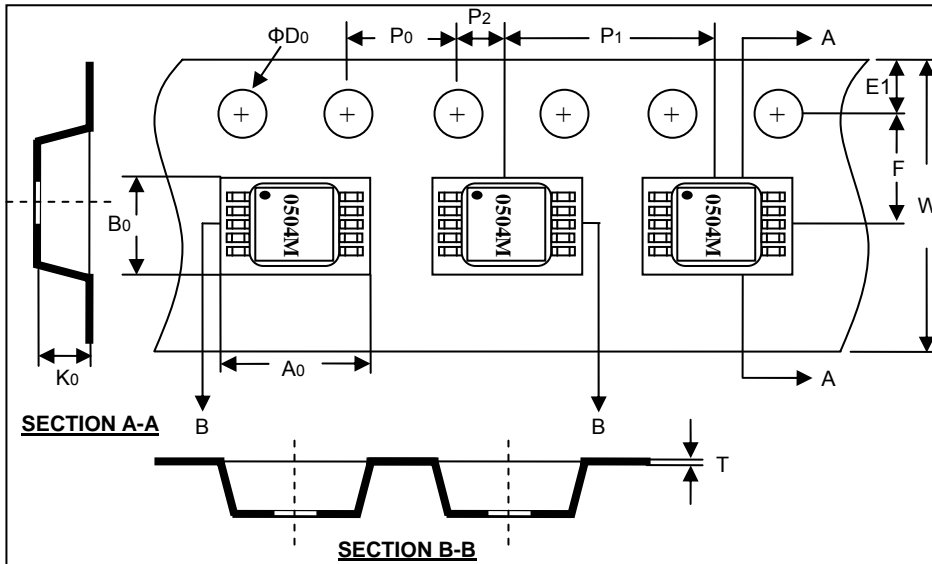
4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

MSOP-10 Dimension Drawing

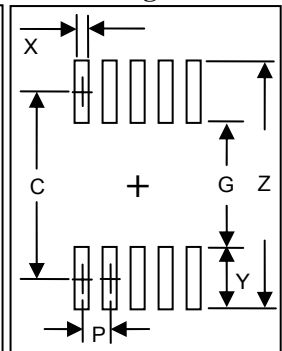


Dim	Dimensions			
	Inches		mm	
	Min	Max	Min	Max
A	0.028	0.038	0.75	0.95
A1	0.002	0.006	0.05	0.15
B	0.007	0.013	0.17	0.33
C	0.007		0.18	
D	0.114	0.122	2.90	3.10
E	0.114	0.122	2.90	3.10
e	0.0196 BSC		0.50 BSC	
H	0.193 BSC		4.90 BSC	
L	0.0137	0.029	0.40	0.70

MSOP-10 Carrier Dimension



Mounting Pattern



Typical		
Dim	MM	Inches
C	4.100	0.161
G	2.500	0.098
P	0.500	0.020
X	0.300	0.011
Y	1.600	0.063
Z	5.700	0.224

Dimensions in mm.

Reel Dia.	Tape Width	A0	B0	K0	T	D0
330mm (13")	12mm	5.20±0.20	3.30±0.10	1.60±0.20	0.30±0.05	1.50±0.10
P0	P1	P2	E1	F	W	
4.00±0.10	8.00±0.10	2.00±0.05	1.75±0.10	5.50±0.05	12.0±0.30	



4 Channel Ultra Low Capacitance Dual-Rail Clamp Array for ESD Protection

Marking Code

Part Number	Device Marking
UMD0504M	0504M

Ordering Information

Part Number	Lead Finish	Qty Per Reel	Reel Size
UMD0504M	Pb-Free	4,000	13 inch

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